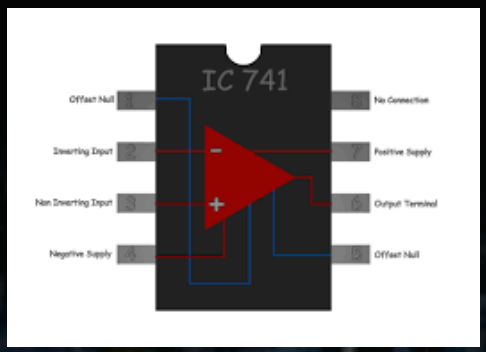
ELECTRONIC DEVICES AND ANALOG ELECTRONICS

Specially Designed for GATE Examination



VOLUME I

by Ram Niwas (IES)

ELECTRONIC DEVICES AND ANALOG ELECTRONICS

VOLUME I

First Edition

2021

ELECTRONIC DEVICES AND ANALOG ELECTRONICS

VOLUME I

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CONTENTS

HOW TO READ THIS BOOK

This book has been designed to meet the requirement of all Electrical, Electronics and Instrumentation Engineers. It is has been written in simple and lucid language so that students from all backgrounds, having little knowledge of English, can understand. It is designed to develop facts and concepts for competitive examinations in India like GATE, IES, PSUs and IAS examinations. The book can be referred for University Syllabus across different countries in the world. Every chapter is followed and prepared after in depth analysis of previous year questions which appeared in these competitive examinations. The focus is mainly on developing concepts along with facts. Each chapter has been followed by previous years fully solved questions of GATE of Electronics, Electrical and Instrumentation Engineering. These questions are helpful for university examination also.

For students studying in B.E./B.Tech

This book would help students studying in B.Tech to prepare for their university examination. In parallel book is equipped to prepare B.Tech students for competitive examinations like GATE and ESE. However, main focus of students of B.Tech should be to develop concepts and then practice question of GATE.

For students preparing for GATE

The theory of this book has been prepared to develop theoretical concepts for those students who are preparing for GATE. Such students should focus on theoretical concepts followed by practicing previous year GATE questions which are given at the end of each chapter along with full solutions. Students first try to solve the question themselves and the refer the solution.

For students preparing for ESE Preliminary

The theory of this book has been prepared for students preparing for ESE both Electrical and Electronics Preliminary and Mains Examinations and IAS Electrical mains examination. However, students preparing for ESE Pre examination should note down factual information and formulas in their notebook in form of brief notes. It helps in quick revision just before the Pre examination. Each chapter has been provided with fully solved questions of ESE Pre for both EE and EC. Students should practice these questions in time bound manner with one question in one minute. It would help to build speed and accuracy. Solutions should be referred only to clarify doubt if any.

For students preparing for ESE Mains and IAS Mains

The students preparing for ESE Mains of EE and EC or IAS Electrical mains should practice questions from all these examination so that they have enough practice questions. However, solutions of these question will be provided in next edition of this book. Such students should not wast much time on reading theory in whole they should relevant portion which are important for mains examination as they have already studied the whole theory while preparing for preliminary stage.

PREFACE TO FIRST EDITION

Chapter 1

Chapter 1 gives an introduction to semi-conducting materials, their types and energy band diagrams. It also describes the electrical properties of semiconductors, their Fermi levels and mechanism of flow of current. This chapter is important for GATE EC, ESE Pre for EE and EC and ESE mains for EC.

Chapter 2

Chapter 2 introduces the PN junctions and their behaviour under forward and reverse biased conditions, components of diode current. It also introduces the diode capacitances and resistances. Different types of diodes and their operational features are also discussed in detail. This topic is important for all the competitive examination of Electrical, Electronics and Instrumentation engineers.

Chapter 3

Chapter 3 Introduces bipolar junction transistors, their characteristics, configurations and current components. It is important topic for understanding of operations of BJT based amplifiers. This chapter is important for GATE examination of EE, EC and ESE pre examinations of EE and EC.

Chapter 4

Chapter 4 Explains MOS Capacitor, Construction and operation of MOSFETs and JFETs. It is important mainly for GATE EC and ESE Pre and mains of EC and EE. This chapter is important for understanding of amplifier circuits based MOSFET and JFETs.

CHAPTERWISE GATE SYLLABUS

Chap.	Topic	Electronics & Comm. Engineering	Electrical Engineering	Instrumentation Engineering
Ch.1	Semiconductors	Energy bands in intrinsic and extrinsic semiconductors, equilibrium carrier concentration, direct and indirect band-gap semiconductors, Carrier transport: diffusion current, drift current, mobility and resistivity, generation and recombination of carriers, Poisson and continuity equations		
Ch.2	Diodes	P-N junction, Zener diode, LED, photo diode and solar cell		Characteristics and applications of diode, Zener diode
Ch.3	Bipolar Junction Transistors	BJT		Characteristics and applications of BJT
Ch.4	Field Effect Transistors	MOSFET & MOS Capacitor		Characteristics and applications of MOSFET
Ch.5	Diodes Circuits	Diode circuits: clipping, clamping and rectifiers.	Simple diode circuits: clipping, clamping, rectifiers	
Ch.6	BJT Biasing & Thermal Stabilization	BJT amplifiers: biasing	Amplifiers: Biasing	
Ch.7	MOSFET Biasing	MOSFET amplifiers: biasing	Amplifiers: Biasing	
Ch.8	Small Signal Analysis of BJT	BJT amplifiers: ac coupling, small signal analysis	Amplifiers: Equivalent circuit	small signal analysis of transistor circuits
Ch.9	Small Signal Analysis of FET	MOSFET amplifiers: ac coupling, small signal analysis	Amplifiers: Equivalent circuit	small signal analysis of transistor circuits

Chap.	Topic	Electronics & Comm. Engineering	Electrical Engineering	Instrumentation Engineering
Ch.-10	Frequency Response	BJT and MOSFET amplifiers : frequency response	Amplifiers: Frequency response	
Ch.11	Multistage Amplifiers			
Ch.12	Compound circuits	BJT and MOSFET amplifiers : Current mirror		
Ch.13	Feedback Amplifiers		Feedback amplifiers	Feedback amplifiers
Ch.14	Differential Amplifiers	BJT and MOSFET amplifiers : differential amplifiers.	BJT and MOSFET Differential Amplifiers	
Ch.15	Operational Amplifiers & its circuits	Op-amp circuits: Amplifiers, summers, differentiators, integrators, active filters, Schmitt triggers and oscillators.	operational amplifiers: characteristics and applications; single stage active filters, Sallen Key, Butterworth, VCOs and timers	Characteristics of ideal and practical operational amplifiers; applications of opamps: adder, subtracter, integrator, differentiator, difference amplifier, instrumentation amplifier, precision rectifier, active filters, oscillators, signal generators, voltage controlled oscillators and phase locked loop, sources and effects of noise and interference in electronic circuited oscillators and phase locked oscillators, signal generators, voltage controlled oscillators and phase locked loop.
Ch.16	Oscillators		Oscillators	
Ch.17	Power Supplies			
Ch.18	Power Amplifiers			

CHAPTERWISE ANALYSIS OF GATE QUESTIONS

Electronics and Communication Engineering : EDC & Analog Electronics

Chap	Topic	2010	2011	2012	2013	2014				2015			2016			2017		2018	2019	2020	2021
						IV	III	II	I	III	II	I	III	II	I	II	I				
Ch.1	Semiconductors	4	1			7	2	3			6	1		2	5		5			1	2
Ch.2	Diodes	2	2		1		3		4			5	4	4	2	4	3	12	10	5	2
Ch.3	BJT and Its Characteristics	2	2			2		1	2	3			2	1		1	1		1	2	
Ch.4	FET and Its Characteristics	2	6	8	5		7	5	4	5	2	4	3	5	4	8	2	3	3	2	2
Ch.5	Diode circuits		4	3	4	1		2	1	3	3	1	3	2		1			5	1	2
Ch.6	Biasing of BJT		2		2		3	1		1			1			1	2				
Ch.7	Biasing of MOSFET																			2	2
Ch.8	Small Signal Analysis of BJT	2		1		7			2		2		4			2	2			2	
Ch.9	Small Signal Analysis of FET	2		1		7			2		2		4			2	2			2	1
Ch.10	Frequency Response	4															1				
Ch.11	Multistage Amplifiers							1						1							
Ch.12	Compoud circuits	1												1					4		
Ch.13	Feedback Amplifiers			2	1		1	1	1								1	1			
Ch.14	Differential Amplifiers							1				2									
Ch.15	Operational Amplifiers & its circuits	3	1	2	3	2	2		6	3	6	4	3	4	8	2	3	4		4	4
Ch.16	Oscillators																				
Ch.17	Power Supplies																			2	
Ch.18	Power Amplifiers																				
	Total Marks	**22**	**18**	**14**	**16**	**26**	**18**	**19**	**22**	**15**	**21**	**17**	**24**	**20**	**19**	**21**	**22**	**20**	**23**	**23**	**15**

Electrical Engineering : EDC & Analog Eectronics

Chap	Topic	2010	2011	2012	2013	2014				2015			2016			2017		2018	2019	2020	2021
						IV	III	II	I	III	II	I	III	II	I	II	I				
Ch.1	Semiconductors																				
Ch.2	Diodes																			2	
Ch.3	BJT and Its Characteristics										1									1	
Ch.4	FET and Its Characteristics																		1	2	
Ch.5	Diode circuits		2	2	4			2			2				3						4
Ch.6	BJT Biasing		2	2							1	1			1	2		2	2	2	1
Ch.7	FET Biasing																				
Ch.8	Small Signal Analysis of BJT									1										1	
Ch.9	Small Signal Analysis of FET																				
Ch.10	Frequency Response of BJT & MOSFET																				
Ch.11	Multistage Amplifiers																				
Ch.12	Compoud circuits																				
Ch.13	Feedback Amplifiers			2	1														1		
Ch.14	Differential Amplifiers																2			2	
Ch.15	Operational Amplifiers & its circuits	1	1	4	3		3	2	3		4	4		3		2	2		2		2
Ch.16	Oscillators																				
Ch.17	Power Supplies																			2	
Ch.18	Power Amplifiers																				
	Total Marks	**1**	**5**	**10**	**8**		**3**	**4**	**5**	**1**	**8**	**5**		**3**	**4**	**4**	**4**	**2**	**6**	**12**	**7**

Instrumentation Engineering : EDC & Analog Eectronics																
Chap	**Topic**	**2010**	**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**	**2022**	**2023**	**2024**
Ch.1	Semiconductors															
Ch.2	Diodes and theirs circuits							3	2		1					
Ch.3	BJT & Its Characteristics															
Ch.4	FET Characteristics and its biasin						2		2							
Ch.5	Diodes Circuits		2	2	4	1	1		1	1	1	3				
Ch.6	BJT Biasing				1	4	2									
Ch.7	FET Biasing															
Ch.8	Small Signal Analysis of BJT		1		1		2				2					
Ch.9	Small Signal Analysis of FET															
Ch.10	Frequency Response of BJT & MOSFET															
Ch.11	Multistage Amplifiers															
Ch.12	Compound circuits	2									2		3			
Ch.13	Feedback Amplifiers															
Ch.14	Differential Amplifiers															
Ch.15	Operational Amplifiers	7	11	2	12	8	4	15	8	7	3		5			
Ch.16	Oscillators								1			9				
Ch.17	Power Supplies															
Ch.18	Power Amplifiers															
Ch.19	Tuned Amplifiers															
Ch.20	Multivibrators															
	Total Marks	**9**	**14**	**4**	**18**	**13**	**11**	**18**	**14**	**8**	**9**	**12**	**8**			

Ch 1 Semiconductors

1.1 Atomic Structure of Materials

The understanding of atomic structure is an important step to under stand the structure of solids including semiconductors. Rutherford found that atoms consists of a nucleus of positive charge consisting protons. The nucleus is surrounded by negatively charged particles called electrons. The number of protons in nucleus is same as the number of electrons. The electrons revolve around the nucleus in closed orbit.

According to Bohr postulates the electrons around the nucleus always occupies discrete energy level. The energy of electron in Joules at n^{th} level is given by,

$$W_n = -\frac{mq^4}{8h^2\varepsilon_o^2}\frac{1}{n^2} \quad (1)$$

where h is plank's constant, m is mass & q is charge of electron and ε_o is dielectric constant of free space.

When atom is exposed to a photon, the electron can shift from one energy level to another level if the energy of photon is equal to energy difference between two energy levels. The electron can again fall back to its normal state by emitting photons having energy equal to the deference in energy levels.

The electrons around the nucleus are located in shells. There are four quantum number associated with an electron in a shell. These quantum numbers are known as n,l,m ans s.

The these quantum numbers are restricted to following integral values,

$n = 1, 2, 3$

$l = 0,1,2,3., (n-1)$

$m = 0, \pm1, \pm2, \pm3 . \pm l$

$s = \pm 1/2$

According to Pauli's exclusion principle no two electrons can have same set of quantum numbers in an atom. All electrons having same value of n belong to same electronic shell identified by K,L,M & N corresponding to n = 1,2,3,4.... The shell are divided in sub-shell corresponding to different value of l and identified by s,p,d,

The atomic number and electronic configurations of important semiconductors are given in below,

Element	Atomic No.	Configuration
C	6	$1s^2 2s^2 2p^2$
Si	14	$1s^2 2s^2 2p^6 3s^2 3p^2$
Ge	32	$1s^2 2s^2 2p^6 3s^2 3p^6 3d^{10} 4s^2 4p^2$
Sn	50	$1s^2 2s^2 2p^6 3s^2 3p^6 3d^{10} 4s^2 4p^6 4d^{10} 5s^2 5p^2$

It is observed that the outer most shell in all the atoms of goup IV has four electrons.

Note : The energy state of the electrons in an atom can be determined by using Schrödinger equation (Schrödinger-equation).

1.2 Bonding in solids

Atoms are rarely found as free and independent units, but usually are linked or bonded to other atoms in some manner as a result of inter-atomic forces. The forces between two atoms or ions is function of distance. This force is repulsive when separation is small and attractive when separation is large. A particular separation the force of repulsion is equal to force of attraction and net force is zero. These bonding forces between the atoms are called chemical bonds and the process of holding them is called ***bonding***. According to strength chemical bonds are grouped in to two groups called primary bonds and secondary bonds. The primary bonds are three types called Ionic, Covalent and Metallic Bonds. **Ionic bond** is a simplest type of primary bond. Ionic bonding forms between two oppositely-charged ions which are produced by the transfer of electrons from one atom to another. The positive and negative ions have a natural attraction from each other, producing a strong bonding force. The ionic bond is said to be *non-directional.* **Covalent bonds** are formed by the *sharing of electrons* between neighboring atoms. In this type of bond, the atoms being linked find it impossible to produce complete shells by electron transfer, but achieve the same goal by electron sharing so that each attain a stable electronic structure. Moreover, the shared negative electrons locate between the positive and negative nuclei to form the bonding link. This also gives *directionality to the covalent bond.* Some of the materials having covalent bond are Carbon , Silicon, Germanium, Gray tin etc. **Metallic Bonds** are exhibited by the elements to the left of the fourth column in the periodic table,having small number of valence electrons. The ***Van der Waals Bonds*** are weak or secondary bonds which can link molecules that posses a non-symmetric distribution of atoms.

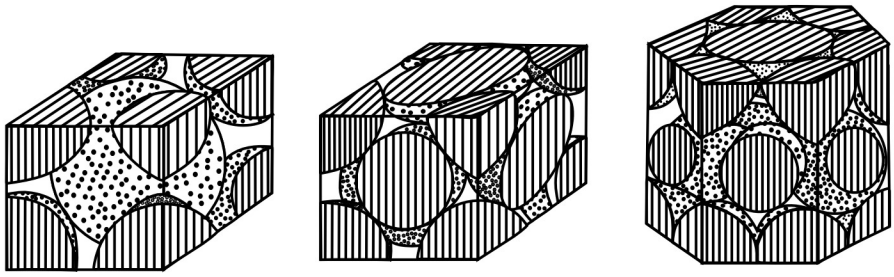
Note : *The Semiconductor atoms of Group-IV exhibits the covents bonds.*

1.3 Crystal Geometry and Structure

A crystal is a solid whose constituents molecules or atoms are arranged in a systematic pattern. In crystalline solids the pattern of atoms is repeated periodically. The solids which are non-crystalline the internal structure is not based on repeated patterns.

Space Lattice

A space lattice is an infinite array of points in three dimensions in which every point has surroundings identical to those of every other point in the array. A unit cell is smallest unit of a space lattice. Space lattices of various materials differ in shape and size of their unit cells. Crystals of most of metals have highly symmetrical structures with closed packed atoms. The most common types of space lattices are Body centered cubic(BCC), Face centered cubic(FCC) and Hexagonal closed packed(HCP) as shown in



(a) BCC (b) FCC (b) HCP

Fig. 1 Unit cells of BCC, FCC and HCP

The basic crystal structure of many important semiconductors is FCC lattice with a basis of two atoms giving rise to the Diamond structure, characteristic of Si, Ge and C in the diamond form. In many compound semiconductors formed with Group III-V compounds, the atoms are arranged in a basic diamond structure but sub-lattices of different atoms are inter-penetrated resulting in a structure called zinc blende structure.

Note : *Si and Ge has FCC lattice and Diamond structure and GaAs has FCC sub-lattices of Ga and As inter-penetrating resulting in zinc blende structure.*

1.4 Energy Band Theory of Crystals

When atoms form crystals, it is found that the energy levels of the inner-shell electrons are not affected appreciably by the presence of the neighboring atoms. However, the levels of the outer-shell electrons are changed considerably, since these electrons are shared by more than one atom in the crystal. The new energy levels of the outer electrons can be determined by means of quantum mechanics and it is found that coupling between the outer-shell electrons of the atoms results in a *band* of closely spaced energy states, instead of the widely separated energy levels of the isolated atom.

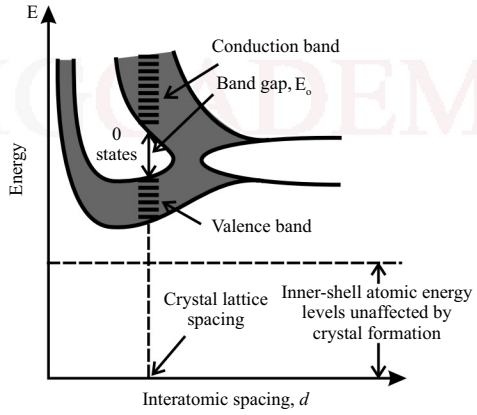


Fig. 2 Splitting of energy levels of isolated atoms to energy bands

The energy band is split into two bands called valence band and conduction band. The valence band consists of empty energy states and conduction band consists of filled energy states. There is an energy gap between the valence and conduction bands called band gap decreases as the atomic

spacing decreases. The band gap (E_g) is measured in electron-volt(eV). One electron-volt is equal to 1.6×10^{-19} Joules.

1.5 Insulators, Semiconductors and metals

A very poor conductor of electricity is called an *insulator;* an excellent conductor is a *metal;* and a substance whose conductivity lies between these extremes is a *semiconductor.* A material may be placed in anyone of these three classes, depending upon its energy-band structure.

Insulators : The materials have large band gap of order of 6eV or more. This large forbidden band separates the filled valence region from the vacant conduction band as shown in Fig.3. In such materials the energy which can be supplied to an electron from an applied field is too small to carry the electron from the filled valence band to vacant conduction band. Since the electron cannot acquire sufficient applied energy, conduction is impossible, and hence they are an *insulator.* Therefore, the resistance of these materials is very high normally of order of mega-ohms.

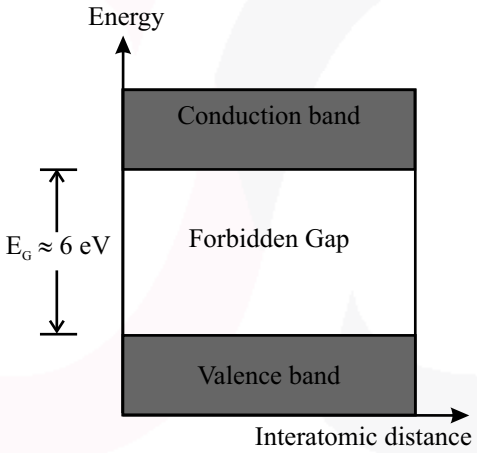


Fig. 3 Energy band structure of insulators

Semiconductors : A substance for which the width of the forbidden energy region is relatively small (~ 1 eV) is called a *semiconductor.* Graphite, a crystalline form of carbon but having a crystal symmetry which is different from diamond, has such a small value of E_G, and it is a semiconductor.

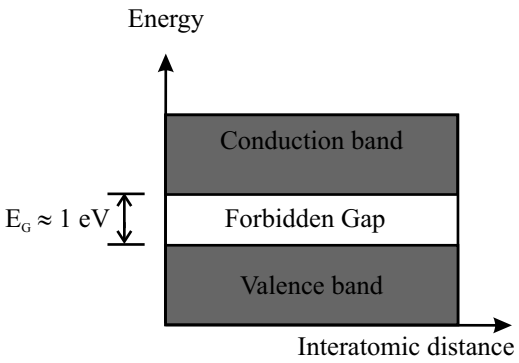


Fig. 4 Energy band structure of semiconductors

The most important practical semiconductor materials are germanium and silicon, which have values of E_G of 0.785 and 1.21 eV, respectively, at 0°K. Energies of this magnitude normally cannot be acquired from an applied field. Hence the valence band remains full, the conduction band empty, and these materials are insulators at low temperatures. However, the conductivity increases with temperature. These substances are known as *intrinsic semiconductors.*

As the temperature is increased, some of these valence electrons acquire *thermal* energy greater than E_G, and hence move into the conduction band. These are now free electrons in the sense that they can move about under the influence of even a small applied field. The insulator has now become slightly conducting; it is a *semiconductor.* The absence of an electron in the valence band is called a *hole.* Since, there is generation of electron and hole pair with increase in temperature, therefore, resistance of semiconductors decreases with increase in temperature. Because of this characteristic semiconductors are said to be having negative temperature coefficient.

If certain impurity atoms are introduced into the crystal, these result in allowable energy states which lie in the forbidden energy gap. These impurity levels also contribute to the conduction. A semiconductor material where this conduction mechanism predominates is called an *extrinsic semiconductor.*

Since the band-gap energy of a crystal is a function of inter-atomic spacing as well as temperature. The band gap decreases with increase in temperature.

Metals : These are the materials in which conduction and valence bands overlap with each other. Therefore, there is no forbidden gap between valance band and conduction band. So all the electrons are free and are in saturated state. A material which contains a partly filled band structure is called a *metal.*

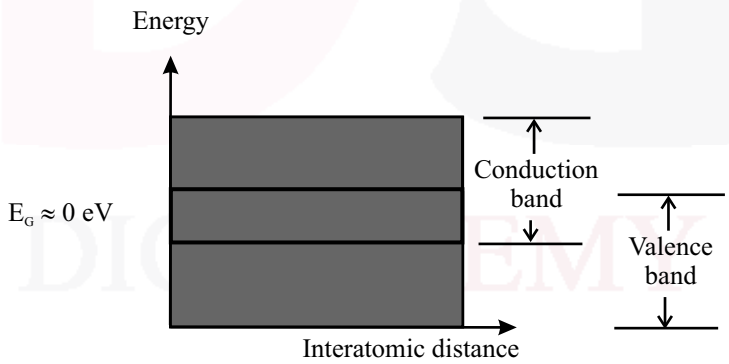


Fig. 5 Energy band structure of metals

Under the influence of an applied electric field the electrons may acquire additional energy and move into higher states. Since these mobile electrons constitute a current, this substance is a conductor and the partly filled region is the conduction band. When temperature of metals is increased the lattice vibrations are increased due to increased thermal agitation so the rate of collision of electrons with lattice sites is also increased. Because of increased collision rate the resistance of metals increases with increase in temperature. Therefore, metals have the positive temperature coefficient.

1.6 Elemental and Compound Semiconductors

The semiconductors are found in column IV and neighboring columns of periodic table. The column IV semiconductors Silicon (Si) and Germanium (Ge) are called elemental semiconductors because they are composed of single type of atoms.

In addition to elemental materials, compounds of Column III and Column V atoms as well as certain combination from Column II and Column VI and from Column make up compound semiconductors. The elemental semiconductor Si is widely used in integrated circuits. The compound semiconductors are mostly used for high speed devices and light emitting or absorption devices. The group III-IV compounds, GaAs, GaP and GaN are commonly used in light emitting diodes (LEDs). The semiconductors and their applications are summarized under,

Semiconductor	Type	Application
Si	Elemental	ICs, Infrared and nuclear radiation detector
Ge	Elemental	Discrete Devices and Infrared and nuclear radiation detector
GaAs	Group III-V	LED, Semiconductor LASER
GaP	Group III-V	LED
GaN	Group III-V	LED
GaAsP		
InGaAsP		
AlGaAs		Semiconductor LASER
InSb	Group III-V	Light Detector
CdSe	Group II-VI	Light Detector
PbTe		Light Detector
ZnS	Group II-VI	Television Screen

Note : Band gap of GaAs is 1.43 eV and Band gap of GaP is 2.3 eV.

1.7 Charge Carriers in Semiconductors

Unlike metal which have only electrons as charge carriers, the semiconductors have two types of charge carriers called ***electrons and holes***. The electrons are available in conduction band and holes are available in the valence band. When a semiconductor atom releases an electron it acquires a positive charge. As semiconductors atoms have semi-stable electronic configuration so they have equal tendency to give away or take electrons. (So, the positive ion of semiconductor can easily take back an electron). Because of this characteristic the positive charge in valence band can shift from one location to another location. Because of this shifting nature of positive charge of semiconductor ion it is called a hole. So, a hole is not a physical particle rather a positive ion of semiconductor atom.

1.8 Intrinsic Semiconductors

These are pure semiconductors having no impurity. The group IV elements of transition table are the examples intrinsic semiconductors. Silicon(Si) and Germanium(Ge) are two most commonly used intrinsic semiconductors. Both Si and Ge are used for fabrication of discrete devices but Si is preferred for IC fabrication because of following advantages,

i. Si is available in abundance
ii. It is possible to provide electrical isolation is insulating layer between components in Si chip.
iii. Dielectric layer of SiO_2 can be easily fabricated on Si chip.
iv. It stable up to higher temperature.
v. It has smaller reverse saturation current.
vi. Higher melting point 1240 °C as compared to 937 °C of Ge.
vii. Larger band gap
viii. Better heat conductivity
ix. Non toxic

1.8.1 Band gap of Si and Ge

A. Germanium, Ge :

Band Gap of Ge, $E_g = 0.785 - 2.23 \times 10^{-4} T$ eV (2)

where T is Temperature in Kelvin

(i) At 0°K, $E_g = 0.785$ eV

(ii) At room temperature of 300° K, $E_g = 0.72$ eV

B. Silicon, Si :

Band Gap of Si, $E_g = 1.21 - 3.6 \times 10^{-4} T$ eV (3)

(i) At 0°K, $E_g = 1.21$ eV

(ii) At room temperature of 300° K, $E_g = 1.12$ eV

Note : *Band gap of semiconductors decreases with increase in temperature.*

Note : *Band gap of some important semiconductors*

Elements	Band gap (in eV)
Ge	0.72
Si	1.12
Ga As	1.43
GaP	2.3
InP	1.35
In Ga As	0.75
Ga Al As	1.8

Example-1

The band gap of silicon at 300 K is

(a) 1.36 eV (b) 1.10 eV

(c) 0.80 eV (d) 0.67 eV

GATE(EC/2003/1M)

Solution: Ans.(b)

The energy band gap in the Si is function of temperature as temperature increases the band gap energy decreases.

$$E_g(T) = 1.21 - 3.60 \times 10^{-4} T \text{ eV}$$

at $T = 300K$

$$E_g(300\text{ K}) = 1.21 - 3.60 \times 10^{-4} \times 300 \text{ eV}$$

$$= 1.102 \text{ eV}$$

Note:- For Ge, $E_g(T) = 0.785 - 2.23 \times 10^{-4} T \text{ eV}$

1.8.2 Carrier Concentration in Intrinsic Semiconductors

The electrons and holes concentrations are equal in intrinsic semiconductors. Mathematically it is given by,

$$n_i^2 = A_o T^3 e^{-E_{go}/kT} \quad (4)$$

Where, E_{go} is the band gap at 0 Kelvin, k is the Boltzmann constant, T is temperature in Kelvin and A_o is a constant.

$$\Rightarrow \quad n_i \propto T^{3/2} \quad (5)$$

Note : *Bolzmann's constant , $k = 8.62 \times 10^{-5}$ eV/°K = 1.38×10^{-23} J/°K*

Note : *From above relation it is clear that the concentration of charge carriers increases with increase in temperature.*

1.8.3 Important Properties of Ge, Si and GaAs Semiconductors

Property	Ge	Si	GaAS
Atomic number	32	14	
Atomic weight, g/cm^3	72.6	28.1	144.63
Dielectric Constant	16	12	13.1
Atoms / cm^3	4.42×10^{22}	5×10^{22}	4.42×10^{22}
n_i at 300 K / cm^3	2.5×10^{13}	1.5×10^{10}	1.79×10^{6}
Intrinsic Resistivity at 300 K , Ω-cm	45	2.3×10^{5}	10^{8}
μ_n cm^2/V-s at 300 K	3800	1300	8500
μ_p cm^2/V-s at 300 K	1800	500	400

Note : Mobility of electrons in GaAs in highest so frequency response of devices made of GaAs is faster.

1.9 Extrinsic Semiconductors

When some substitutional impurities are added to intrinsic semiconductors the resulting semiconductors are called extrinsic semiconductors. The extrinsic semiconductors can be either n-type or p-type depending on the type of impurity added to them.

1.9.1 n-type Semiconductors

The n-type of semiconductors are obtained by doping with penta-valent impurities from group-V atoms. These impurities are known as n-type or donor type impurities. The impurities from group V have tendency to donate one electron from their outer shell in order to acquire the electronic configuration of group-IV semiconductors. The outer energy level of these impurities lies close to the conduction band of the semiconductors as shown in Fig.6 . So, when small amount of energy is supplied to semiconductor the electrons are transferred from donor level to conduction band leaving behind the positive ions of impurity atoms.

The ions of impurity atoms have no tendency to take electrons so they form positive bound charge. Therefore, the concentration of electrons in the conduction band becomes more than the intrinsic level depending on the donor concentration.

Examples of donor impurities are ***P, As*** and ***Sb***. Phosphorus is most commonly used donor impurity.

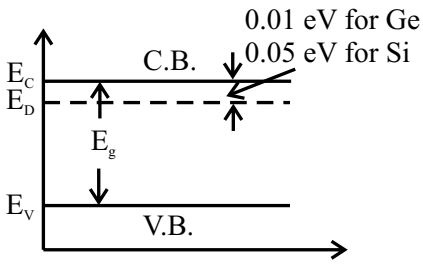


Fig. 6 Energy band diagram of n-type semiconductors

Note : *The concentration of holes in n-type semiconductors falls below the intrinsic level due to increased recombination rate.*

1.9.2 p-type Semiconductors

The p-type of semiconductors are obtained by doping with impurities from group-III atoms. These impurities are known as p-type or acceptor type impurities. The impurities from group-III have tendency to accept one electron from their neighboring atom in order to acquire the electronic configuration of semiconductors. The outer energy level of these impurities lies close to the valence band of the semiconductors as shown in Fig.7. So, when small amount of energy is supplied to semiconductor the electrons from valence band are transferred to acceptor level. Leaving behind large number of holes in valence band and negative ions at acceptor level.

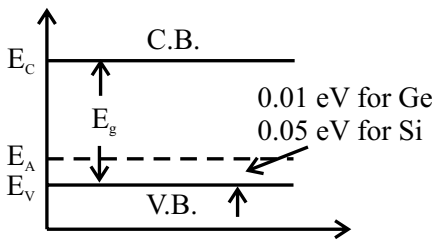


Fig. 7 Energy band diagram of p-type semiconductors

The ions of impurity atoms have no tendency to give away the electrons so they form negative bound charge. The concentration of holes in the valence band becomes more than the intrinsic level depending on the acceptor concentration.

Examples of acceptor impurities are ***B, Al, Ga*** and ***In***. Boron is most commonly used acceptor impurity.

Note : *The concentration of electrons in p-type semiconductors falls below the intrinsic level due to increased recombination rate.*

Note : *i) An extrinsic semiconductor having both types of impurities behaves like n-type material when donor concentration is more than acceptor concentration [i.e. $N_D > N_A$]*

ii) An extrinsic semiconductor having both types of impurities behaves like p-type material when acceptor concentration is more than donor impurity [i.e. $N_A > N_D$].

iii) An extrinsic semiconductor having both types of impurities behaves like intrinsic semiconductor when when acceptor concentration is equal to the donor impurity $N_A = N_D$.

In III-V semiconductors, the impurity from Column VI of the Periodic Table behaves as donor when it occupies the sites of Column V atoms. For example S, Se and Te are donors in GaAs since they replace the As atom and provide an extra electron as compared to As atom. Similarly, impurity from Column II of Periodic Table behaves as acceptor when it occupies the sites of Column III atom in III-V semiconductor. For example Be, Zn & Cd are acceptors in GaAs since they replace the Ga atom and take an electron from Ga atom.

A more ambiguous situation arises when III-V compounds are doped with Si or Ge. Si and Ge can behave acceptor or donor in III-V compound depending on the site occupied by the Si and Ge. When Si atom occupies the site of group -III atom it acts as donor because it has an extra electron as compared to group-III atom and when Si atom occupies the site of group V atom it acts like acceptor because it takes one electron from group V atom. For example when GaAs is doped with Si the resulting semiconductor is n-type when Si occupies the site of Ga atom and it is p-type when Si atom occupies the site of As atom.

Note : *The electron density 'n' in a Si sample doped with a fixed number of group-V impurities increases first due to electron-hole pair generation then becomes constant when electron hole pair generation reaches at saturation and then again increases due to ionization with increase in temperature.*

Note : i. Low level doping in Silicon and Germanium corresponds to impurity of the order of 1 part in 10^9 .

ii.. Medium doping in Silicon and Germanium corresponds to impurity of the order of 1 part in 10^6 .

iii. High level doping in Silicon and Germanium corresponds to impurity of the order of 1 part in 10^3 .

iv. 1 part in 10^8 donor type impurity added to Ge improves its conductivity at 30° C by a factor 12.

1.9.3 Charge Balance Equations of Extrinsic Semiconductors

A semiconductor is always electrically neutral irrespective of impurities in the semiconductor. So, the total positive charge of semiconductor is equal to the total negative charge. The charge balance equations for extrinsic semiconductors equations are as follows,

i. For n-type semiconductor,

$$n = N_D + p \quad (6)$$

Where, n is electron concentration, p is holes concentration and N_D is donor concentration.

ii. For p-type semiconductor,

$$p = N_A + n \quad (7)$$

Where, N_A is acceptor concentration.

iii. For semiconductor with both types of impurities,

$$N_D + p = N_A + n \quad (8)$$

1.10 Law of Mass Action

According to law of mass action the product of electrons and holes concentration in a extrinsic semiconductor is given by,

$$np = n_i^2 \quad (9)$$

where n is concentration of electrons, p is concentration of holes and n_i is intrinsic concentration.

Case-I : Law of mass-action for n-type materials

$$p_n n_n = n_i^2 \quad (10)$$

Where, n_n is concentration of electrons and p_n is concentration of holes.

For n-type materials concentration of electrons is almost equal to the donor concentration.

So, $n_n \approx N_D$.

$\Rightarrow$ $N_D p_n = n_i^2$

$\Rightarrow$ $$p_n = \frac{n_i^2}{N_D} \quad (11)$$

Case-II: Law of mass-action for p-type materials

$$p_p n_p = n_i^2 \quad (12)$$

Where, p_p is concentration of holes and n_p is concentration of electrons .

For p-type materials concentration of electrons is almost equal to the donor concentration.

So, $p_p \approx N_A$.

$\Rightarrow$ $N_A n_p = n_i^2$

$\Rightarrow$ $$n_p = \frac{n_i^2}{N_A} \quad (13)$$

Case-III: Law of mass-action for compensated semiconductors with both types of impurities

When semiconductor is doped with both types of impurity resultant semiconductor is called compensated semiconductor. It may be either p-type or n-type depending on level of doping with acceptor and donor impurities. Such type of semiconductors having both types of impurities are called compensated semiconductors.

Case-A: $N_D > N_A$

Then resultant material is n-type with,

$$n_n \approx N_D - N_A \quad (14)$$

And $$p_n = \frac{n_i^2}{N_D - N_A} \quad (15)$$

Case-B: $N_A > N_D$

Then resultant material is p-type with,

$$p_p \approx N_A - N_D \quad (16)$$

And

$$n_p = \frac{n_i^2}{N_A - N_D} \quad (17)$$

Example : 2

A silicon bar is doped with donor impurities $N_D = 2.25 \times 10^{15}$ atoms / cm^3. Given the intrinsic carrier concentration of silicon at T = 300 K is $n_i = 1.5 \times 10^{10}\ cm^{-3}$. Assuming complete impurity ionization, the equilibrium electron and hole concentrations are

(a) $n_0 = 1.5 \times 10^{16}\ cm^{-3}$, $p_0 = 1.5 \times 10^{5}\ cm^{-3}$ (b) $n_0 = 1.5 \times 10^{10}\ cm^{-3}$, $p_0 = 1.5 \times 10^{15}\ cm^{-3}$

(c) $n_0 = 2.25 \times 10^{15}\ cm^{-3}$, $p_0 = 1.5 \times 10^{10}\ cm^{-3}$ (d) $n_0 = 2.25 \times 10^{15}\ cm^{-3}$, $p_0 = 1 \times 10^{5}\ cm^{-3}$

GATE(EC-II/2014/1M)

Solution : Ans (d)

The concentration of electrons in n-type semiconductors,

$$n_n \approx N_D = 2.25 \times 10^{15}\ cm^{-3}$$

The concentration of holes in n-type semiconductors,

$$p_n = \frac{n_i^2}{N_D}$$

$$\Rightarrow \quad p_n = \frac{\left(1.5 \times 10^{10}\right)^2}{2.25 \times 10^{15}} = 1 \times 10^{5}\ cm^{-3}$$

Example : 3

Consider a silicon sample doped with $N_D = 1 \times 10^{15}/cm^3$ donor atoms. Assume that the intrinsic carrier concentration $n_i = 1.5 \times 10^{10}/cm^3$. If the sample is additionally doped with $N_A = 1 \times 10^{18}/cm^3$ acceptor atoms, the approximate number of electrons/cm^3 in the sample, at T = 300 K, will be_____ .

GATE(EC-IV/2014/2M)

Solution : Ans. (224.9 to 225.1)

When material is doped with both types of impurity resultant material may be either p-type or n-type depending on level of doping with acceptor and donor impurities.

Case-I: $N_D > N_A$

Then resultant material is n-type with,

$$n_n \approx N_D - N_A$$

and

$$p_n = \frac{n_i^2}{N_D - N_A}$$

Case-II: $N_A > N_D$

Then resultant material is p-type with,

$$p_p \approx N_A - N_D$$

and $$n_p = \frac{n_i^2}{N_A - N_D}$$

Given, $N_D = 1 \times 10^{15}/cm^3$, $N_A = 1 \times 10^{18}/cm^3$

Since $N_A > N_D$, therefore given sample is p-type.

So the concentration of electrons in the sample will be,

$$n_p = \frac{(1.5 \times 10^{10})^2}{1 \times 10^{18} - 1 \times 10^{15}} = 225$$

1.11 Direct and Indirect Band Gap Semiconductors

Direct Band-gap semiconductors :

These are the semiconductor materials in which electrons from excited state in conduction band (C.B.) jump directly to valence band (V.B) are called direct band semiconductors.

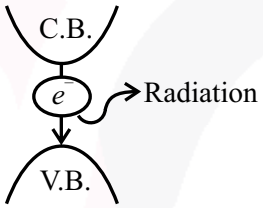


Fig. 8 Direct band gap semiconductor

While jumping from conduction band to valence band the electron lose energy, equal to the band gap, in the form of radiation. So, the energy of radiation emitted by semiconductor atom is equal to the band gap of semiconductor. Mathematically,

$$h\nu = E_g \quad (18)$$

Where , h is planks constant and *v is* frequency of radiation

The frequency radiation is related to velocity of light as under,

$$\nu = \frac{c}{\lambda} \quad (19)$$

Where, λ is wavelength of radiation and c is velocity of light

From equations (18) and (19), we have,

$$\frac{hc}{\lambda} = E_g$$

$$\Rightarrow \quad \lambda = \frac{hc}{E_g} \quad (20)$$

Planck's constant = 6.626×10^{-34} Js and velocity of light, $c = 3 \times 10^8$ m/s

$$\Rightarrow \quad \lambda = \frac{12400}{E_g} \text{Å} \quad (21)$$

Where E_g is measured in eV and 1 Å = 10^{-10} m

The Direct band-gap materials are used for fabrication of LEDs and LASER. Gallium Arsenide (GaAs) is typical example of direct band gap semiconductor used for fabrication of light emitting diodes(LEDs).

Indirect Band-gap semiconductors

The semiconductors in which electrons from conduction band do not jump directly to valence band rather first jump from conduction band to some intermediate energy level called defect level and then from intermediate energy level to valence band, are called indirect band gap semiconductors. In indirect band gap semiconductors the energy of electron is lost in the form of heat to the lattice rather than as an emitted photon.

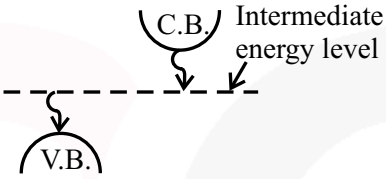


Fig. 9 Indirect band gap semiconductor

Silicon and Germanium are typical examples of indirect band-gap semiconductors.

Note : *GaP is an example of indirect band gap semiconductor but it is used for fabrication of LEDs.*

Note : ***Material***	***Colour emitted by LEDs***
GaAs	*Infrared*
$GaAs_{0.35}P_{0.65}$	*Red*
$GaAs_{0.15}P_{0.85}$	*Yellow*
GaP	*Green-Red*
SiC	*Blue*

1.12 Electrical Properties of Semiconductors

1.12.1 Conductivity

The conductivity of semiconductors is given by,

$$\sigma = ne\mu_n + pe\mu_p \qquad (22)$$

Where, e is electronic charge, n is concentration of electrons, p is concentration of holes, μ_n is mobility of electrons and μ_p is mobility of holes.

Case-I : *Conductivity of intrinsic semiconductors:*

For intrinsic semiconductor, $n = p = n_i$

$$\Rightarrow \quad \sigma = n_i e(\mu_n + \mu_p) \qquad (23)$$

Case-II : *Conductivity of n-type semiconductors:*

For n-type semiconductors, $n >> p$ and $n_n \approx N_D$

$$\Rightarrow \quad \sigma \approx N_D e\mu_n \tag{24}$$

Case-III : *Conductivity of p-type semiconductors:*

For n-type semiconductors, $p >> n$ and $p_p \approx N_A$

$$\Rightarrow \quad \sigma \approx N_A e\mu_p \tag{25}$$

Case-IV : *Conductivity of compensated semiconductors*

For $N_D > N_A$, $\quad \sigma \approx (N_D - N_{A)} e\mu_n$

For $N_A > N_D$, $\quad \sigma \approx (N_A - N_{D)} e\mu_p$

1.12.2 Mobility

Mobilities of electrons and holes are given by,

$$\mu_n = \frac{e\tau_n}{m_n} = \frac{q\tau_n}{m_n} \tag{26}$$

And

$$\mu_p = \frac{e\tau_p}{m_p} = \frac{q\tau_p}{m_p} \tag{27}$$

Where, τ_n is average collision time electrons, τ_p is average collision time of holes, m_n is effective mass of electrons and m_p is effective mass of hole.

Mobility of Semiconductors as a function of Temperature **:**

$$\mu \propto T^m ; \text{ for } 100\ K < T < 400\ K \tag{28}$$

Where, m is a constant.

i. For Si : m = 2.5 for electrons and 2.7 for holes

ii. For Ge : m = 1.66 for electrons and 2.33 for holes

So, the mobility of charge carriers reduces with increase in temperature and Mobility and conductivity of Si is more sensitive to temperature variation then Ge.

Mobility of Semiconductors as a function of Electric field :

The variation of mobility of charge carriers depends on the range of electric field as under,

μ = constant ; for $E < 10^3$ V/cm

$\mu \propto E^{-1/2}$; for 10^3 V/cm $< E < 10^4$ V/cm

$\mu \propto E^{-1}$; for $E > 10^4$ V/cm

Note : *Mobility of electrons almost double of mobility of holes i.e.* $\mu_n = 2\mu_p$

Note : *Mobility of electrons and holes for Ge and Si*

Mobility	***Ge***	***Si***
μ_n	3800 cm^2/V-s	1300 cm^2/V-s
μ_p	1800 cm^2/V-s	500 cm^2/V-s

Note : *Mobility is function of average time, type of materials, temperature (T), electric fields and type of carrier.*

i) Average collision time *ii) Type of materials* *iii) Temperatures*

iv) Electric fields *v) Type of carriers*

1.12.3 Drift velocity

The motion of charge carriers under the influence of electric field is called drifting. The drift velocity

of charge carriers is given by,

$$v_d = \mu E \quad (29)$$

The drift velocity of electrons changes with applied field depending on the range of electric field as shown below,

i) $v_d \propto E$ for $E < 10^3$ V/cm

ii) $v_d \propto E^{-1/2} \times E$; for 10^3 V/cm $< E < 10^4$ V/cm

$\Rightarrow$ $v_d \propto E^{1/2}$

iii) $v_d \propto$ constant ; for $E > 10^4$ V/cm

1.12.4 Effect of temperature on conductivity of Semi-conductors

Conductivity of semiconductors is given by ,

$$\sigma = ne\mu_n + pe\mu_p \quad (30)$$

or

$$\sigma = \frac{ne^2\tau_n}{m_n} + \frac{pe^2\tau_p}{m_p} \quad (31)$$

When temperature of semiconductor is increased there is increase in thermal vibrations of lattice ions and the average collision time of electrons with lattice ions is reduced, which results in decrease in mobility. The decrease mobility results in decrease in conductivity. But the concentration of charge carrier increases with increase in temperature and hence the conductivity increase. The increase in conductivity due to increase in carrier concentration is much more than the decrease in conductivity due to decrease in mobility. Therefore, there is net decrease in resistivity of semiconductors with increase in temperature. Because of this characteristics, the semiconductors are said to be having **negative** temperature coefficients**.**

In extrinsic semiconductor the concentration of charge carrier is at almost saturation level when doping level is very high. In such semiconductors the decrease in conductivity due decrease in mobility is more than increase in conductivity due to increase in temperature. Such semiconductors have positive temperature coefficient transistor is one such semiconductor device having positive temperature coefficient.

Note : *At absolute zero all the electrons from conduction band fall-back to valance band and hence the concentration of free charge carrier reduces to zero. Therefore the conductivity of the semiconductor is zero at absolute zero (i.e. 0 K).*

Note : *A concentration of charge carriers in heavily doped semiconductor reaches at saturation level and materials starts behaving like metals. In such semiconductors the decrease in conductivity is more due to decrease in mobilty of charge carriers. So, heavily doped semiconductors may have positive temperature co-efficient.*

Note : **Effect of temperature on conductivity of pure metal or metals**

The conductivity and mobility of pure metals are given by,

$$\sigma = ne\mu \; ; \; \mu = \frac{e\tau}{m_n} \quad (32)$$

In pure metals the electrons are always in saturation state, therefore conductivity depends on

mobility of electrons only. With increase in temperature, there is increase in thermal vibrations of lattice atoms which results in reduction of average collision time of electrons which in turn reduces the mobility. The reduction in mobility with increase in temperature results in reduction in conductivity or increase in resistivity. Because of this characteristic metals are said to be having positive temperature coefficients. At absolute zero the lattice vibrations in metals ceases and there is no collision of electrons with lattice sites. Therefore, there is no obstruction path of flow of electrons. So, the resistivity of the metal is zero at absolute zero (i.e. 0 ^{o}K).Because of zero resistance at absolute zero the metals behave like superconductor at absolute zero.

Example 4

An n-type silicon bar 0.1 cm long and 100 μm^2 in cross sectional area has a majority carrier concentration of $5\times 10^{20}/m^3$ and the carrier mobility is 0.13 m^2/V-s at 300 K. If the charge of an electron is 1.6×10^{-19} coulomb, then the resistance of the bar is

(a) 10^6 ohm (b) 10^4 ohm

(c) 10^{-1} ohm (d) 10^{-4} ohm

GATE(EC/2003/2M)

Solution : Ans.(a)

Conductivity of extrinsic semiconductors,

$$\sigma = e(p\mu_p + n\mu_n)$$

for n-type semiconductors, n >> p

$$\therefore \quad \sigma \approx ne\mu_n$$

$$\Rightarrow \quad \sigma \approx 5\times 10^{20}\times 1.6\times 10^{-19}\times 0.13 = 10.4$$

$$\Rightarrow \quad \rho = \frac{1}{\sigma} = \frac{1}{10.4} = 0.0962\,\Omega - m$$

Resistance of bar, $R = \rho \times \frac{\ell}{a}$

Given, l = 0.1 c.m. , a = 100 μm^2

$$\Rightarrow \quad R = 0.0962 \times \frac{0.1\times 10^{-2}}{100\times 10^{-12}}\Omega$$

$$\Rightarrow \quad R = 0.962\ M\Omega \approx 10^6\ \Omega$$

Example 5

The resistivity of a uniformly doped n-type silicon sample is 0.5 Ω-cm. If the electron mobility (μ_n) is 1250 cm^2/V-sec and the charge of an electron is 1.6×10^{-19} Coulomb, the donor impurity concentration (N_D) in the sample is

(a) $2\times 10^{16}/cm^3$ (b) $1\times 10^{16}/cm^3$

(c) $2.5\times 10^{15}/cm^3$ (d) $2\times 10^{15}/cm^3$

GATE(EC/2004/2M)

Solution : Ans.(b)

Conductivity of extrinsic semiconductors,

$$\sigma = e(p\mu_p + n\mu_n)$$

for n-type semiconductors, n >> p

$$\therefore \quad \sigma \approx ne\mu_n$$

$$n = \frac{\sigma}{e\mu_n} = \frac{1}{\rho e\mu_n}$$

$$\Rightarrow \quad n = \frac{1}{0.5\times1.6\times10^{-19}\times1250} = 10^{16}/cm^3$$

for n-type semiconductors, $N_D \approx n$

$$\therefore \quad N_D = 10^{16}/cm^3$$

Example 6

A heavily doped n-type semiconductor has the following data:

Hole-electron mobility ratio : 0.4

Doping concentration : 4.2×10^8 atoms/m^3

Intrinsic concentration: 1.5×10^4 atoms / m^3

The ratio of conductance of the n-type semiconductor to that of the intrinsic semiconductor of same material and at the same temperature is given by

(a) 0.00005 (b) 2,000

(c) 10,000 (d) 20,000

GATE(EC/2006/2M)

Solution : Ans.(d)

Given, $N_D = 4.2 \times 10^8$ atoms/m^3, $n_i = 1.5 \times 10^4$ atoms/m^3 and $\frac{\mu_p}{\mu_n} = 0.4$

$$\Rightarrow \quad \mu_p = 0.4\,\mu_n$$

Electrical conductivity of intrinsic semiconductors,

$$\sigma_i = n_i e(\mu_p + \mu_n) = 1.4\ n_i e\mu_n \qquad \text{(i)}$$

Conductivity of extrinsic semiconductors,

$$\sigma_e = e(p\mu_p + n\mu_n)$$

for n-type semiconductors, n >> p & $n \approx N_D$

$$\therefore \quad \sigma_n \approx N_D e\mu_n \qquad \text{(ii)}$$

from equation (i) & (ii),

$$\frac{\sigma_n}{\sigma_i} = \frac{N_D e\mu_n}{1.4 n_i e\mu_n} = \frac{N_D}{1.4 n_i}$$

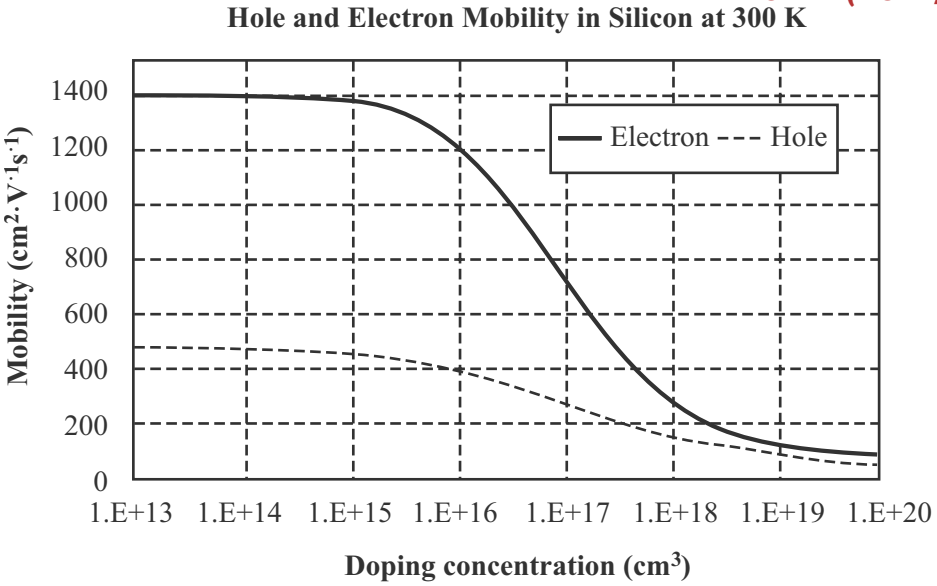
$$\frac{\sigma_n}{\sigma_i} = \frac{4.2\times10^8}{1.4\times1.5\times10^4} = 20000$$

Example 7

A piece of silicon is doped uniformly with phosphorous with a doping concentration of $10^{16}/cm^3$. The

expected value of mobility versus doping concentration for silicon assuming full dopant ionization is shown below. The charge of an electron is 1.6×10^{-19} C. The conductivity (in S cm^{-1}) of the silicon sample at 300 K is

GATE(EC-II/2015/1M)



***Solution* :Ans. (1.8 to 2.0)**

The conductivity of extrinsic semiconductors is given by,

Conductivity of extrinsic semiconductors,

$$\sigma = e(p\mu_p + n\mu_n)$$

The given sample is doped with phosphorous so the resulting material is n-type semiconductor.

For n-type semiconductors, $n >> p$ & $n \approx N_D$

$$\therefore \quad \sigma \approx N_D e\mu_n$$

Given, doping concentration of donor,

$$N_D = 10^{16}/cm^3$$

From the given curve the electron mobility for doping concentration of can be obtained as ,

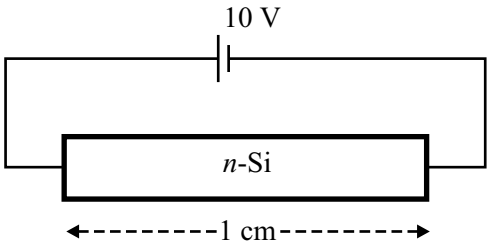
$$\mu_n = 1200\ cm^2V^{-1}s^{-1}$$

$$\therefore \quad \sigma \approx 10^{16} \times 1.6 \times 10^{-19} \times 1200$$

$$\Rightarrow \quad \sigma \approx 1.92\ S\ cm^{-1}$$

Example 8

A dc voltage of 10 V is applied across an *n*-type silicon bar having a rectangular cross-section and a length of 1 cm as shown in figure. The donor doping concentration N_D and the mobility of electrons μ_n are 10^{16} cm^{-3} and 1000 cm^2 V^{-1} s^{-1}, respectively. The average time (in μs) taken by the electrons to move from one end of the bar to other end is ....



GATE(EC-II/2015/2M)

Solution : Ans.(95 to 105)

Donor concentration, $N_D = 10^{16}\ cm^{-3}$

Mobility of electron, $\mu_n = 1000\ cm^2/V\text{-}sec$

Length of bar $L = 1 c.m.$

Electric field inside the bar, $E = \frac{V}{L} = \frac{10}{1} = 10$

Draft velocity of electrons, $v_d = \mu_n E = 1000 \times 10 = 10^4$ c.m./s

Average time taken by electron to move from, one end to another end,

$$t = \frac{L}{v_d} = \frac{1}{10^4} = 10^{-4}\ s = 100\ \mu s$$

1.12.5 Four Point Probe Method

In four point probe method, used to determine the sheet resistance of semiconductor epitaxial layer, inner two probes are voltage probes and outer two probes are current probes. Current is passed through outer probes and voltage is measured across the inner probes. This method eliminate metal to semiconductor contact resistance.

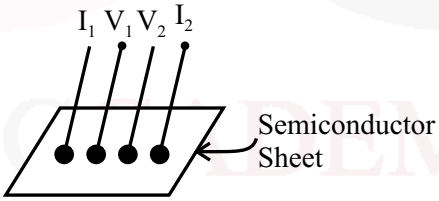


Fig. 10 Four point probe method

Where I_1 & I_2 are current probes and V_1 & V_2 are voltage probes.

The layer's resistance measured with four point probe method is given by,

$$\rho = 4.53\frac{V}{I}\ \text{ohm/square} \qquad (33)$$

Where, V is voltage measured between voltage terminals and I is current passed through current probes.

Example 9

A four-point probe method is used to evaluate the sheet resistance of a semiconductor epitaxial layer.

If a probe current of 10 mA produces a voltage drop of 0.22 V between the inner probes, then the sheet resistance of the layer is

(a) 100 Ω/square (b) 215 Ω/square

(c) 572 Ω/square (d) 1000 Ω/square

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***Solution : Ans.*(a)**

In four point probe method used to determine the sheet resistance of semiconductor epitaxial layer inner two probes are voltage terminals and outer two probes are current terminals. Current is passed through outer probes and voltage is measured across the inner probes. This method eliminate metal to semiconductor contact resistance.

The layer's resistance measured with four point probe method is given by,

$$\rho = 4.53\frac{V}{I}$$

$$\Rightarrow \quad \rho = 4.53 \times \frac{0.22}{10 \times 10^{-3}}$$

$$\Rightarrow \quad \rho = 99.66 \quad \Omega/\text{square}$$

1.12.6 Conductivity Modulation

The conductivity of a semiconductor can be increased by increasing the carrier concentration. The carrier concentration can be increased by generating the electron hole pairs. The electron-hole pairs can be generated by adopting any of the following techniques,

i) By raising the temperature by heating the material.

ii) By illumination with light of suitable wavelength.

iii) By the bombardment of particles such as electrons, α-particles

iv) By exposing to X-rays.

Device Based on principle of conductivity modulation

i) Thermistors : *Thermistor is semiconductor device based on change of resistance of semiconductors due to heating. It has a negative temperature co-efficient. Thermistors are made of sintered mixture of metal oxides such as NiO,Mn_2O_3 and Co_2O_3. Silicon and germanium are not used for construction of thermistors because they are sensitive to impurities. They are used for temperature sensing, thermal relays, thermometry and temperature compensation.*

ii) Sensistor : *It is a semiconductor device with heavy doping level and positive temperature coefficient. It is used for temperature compensation.*

iii) Photo conductors : *These are the semiconductor devices which are based on principle of change in conductivity of semiconductors due to illumination.*

Photoelectric effect :

When a monochromatic light of a frequency more than some limiting frequency is incident on the surface of material such that the electrons comes out the surface of material, the effect is called photoelectric effect. The minimum energy of light required for the photoelectric effect is called work function of material. The energy excess of work function determines the kinetic energy of the photo

electron. The intensity of incident light determines the number of electrons coming out of the surface and frequency of incident light determines kinetic energy of electron emitted from the surface.

The kinetic energy of electron emitted from surface of the material due to photoelectric effect is given by,

$$\frac{1}{2}mv^2 = E - E_W \tag{34}$$

Where m is mass of electron , v is velocity of emitted photoelectrons, $E\ (= hf)$ is energy of incident photon and $E_W\ (= hf_o)$ is work function of the material.

The work function of a metal is defined as minimum amount of energy to be supplied to fast moving electron to bring it out of surface of the metal at 0 °K.

Mathematically, work function is defined as,

$$E_W = E_B - E_F \tag{35}$$

Where E_B is potential barrier of metal and E_F is Fermi level. The potential barrier is minimum potential energy possessed by an electron to come out of the surface of the metal.

1.13 Generation and Recombination of Charge Carriers

Consider a n-type semiconductor bar uniformly illuminated with a light of suitable wavelength.

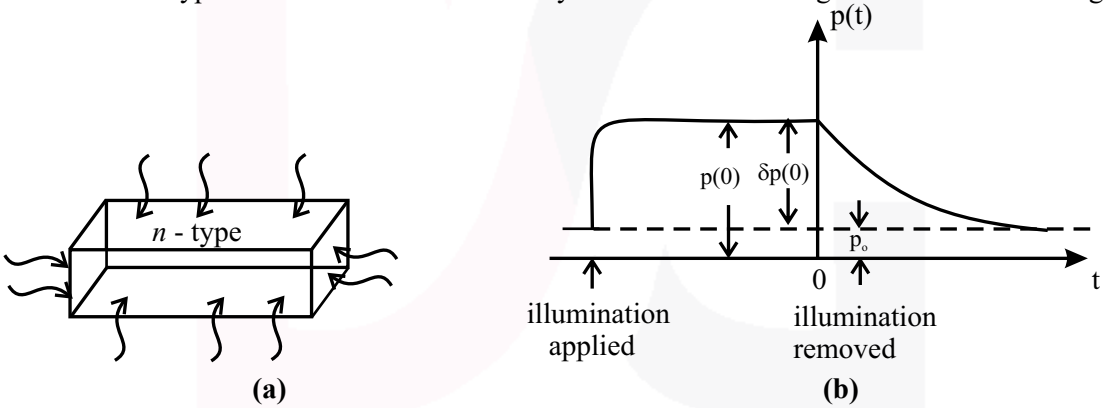

Fig. 11 (a) Uniformly illuminated type semiconductor bar (b) Hole concentration during generation and recombination

The generation and recombination is continuous phenomenon in semiconductors. At thermal equilibrium when no illumination is applied, the generation rate is equal to the recombination rate and concentration of minority charge carriers holes is at level p_o. After illumination, the generation rate becomes more than recombination rate and concentration of charge carriers increases above the steady state level (p_o) as shown in Fig.11b. Under illumination also the concentration reaches at steady state level of p(0) with excess hole concentration of δp(0) above the steady level of p_o. After removal of illumination the rate of recombination becomes more than the generation rate and concentration of holes decrease exponentially from the steady state level of p(0). The percentage change of concentration of minority carriers (i.e. holes) is very large as compared to majority carriers(i.e. electrons), therefore variation of holes is considered for mathematical analysis. However, same analysis holds good for concentration of majority carriers electrons also. The variation of concentration of holes is discussed as follows,

Case-I: After application of illumination

After application of uniform illumination electron-hole pairs are generated due to thermal agitation as well as due to photo-emission. Let g_{op} is rate of optical generation rate and g_o is thermal generation rate and R is recombination rate.

The increase of hole concentration per second can be given by,

$$\frac{dp(t)}{dt} = g_{op} + g_o - R \tag{36}$$

Where, $R = \frac{p}{\tau_p} = \frac{\delta p + p_o}{\tau_p} = \frac{\delta p}{\tau_p} + \frac{p_o}{\tau_p}$ (36a)

In above relation of R, $\delta p/\tau_p$ represents the rate of recombination of excess minority carriers and p_o/τ_p is recombination rate at thermal equilibrium. Here, τ_p represents average life time of holes.

When sample is in under equilibrium state after illumination, $\frac{dp}{dt} = 0$

$$\Rightarrow \quad g_{op} + g_o - \frac{p(0)}{\tau_p} = 0$$

$$\Rightarrow \quad g_{op} + g_o = \frac{p(0)}{\tau_p} = \frac{\delta p(0) + p_o}{\tau_p} = \frac{\delta p(0)}{\tau_p} + \frac{p_o}{\tau_p} \tag{37}$$

Here, $\delta p(0)$ is excess minority carrier concentration above thermal equilibrium at steady state after illumination and p_o is minority carrier concentration under thermal equilibrium when no illumination is applied.

From above equation, the rate of generation of minority carriers under thermal equilibrium is given by,

$$\boxed{g_o = \frac{p_o}{\tau_p}} \tag{38}$$

The optical generation rate of excess minority carriers due to illumination is given by,

$$\Rightarrow \quad \boxed{g_{op} = \frac{\delta p(0)}{\tau_p}} \tag{39}$$

Concentration of excess minority carriers,

$$\delta p = p - p_o$$

Differentiating above equation w.r.t. time, we have,

$$\Rightarrow \quad \frac{d(\delta p)}{dt} = \frac{d(p - p_o)}{dt} = \frac{dp}{dt}$$

From equation (36), (36a), (37) and above relation, we have,

$$\frac{d(\delta p)}{dt} = \frac{\delta p(0)}{\tau_p} - \frac{\delta p}{\tau_p}$$

Solution of above equation gives the concentration of excess minority carriers after illumination,

$$\boxed{\delta p(t) = \delta p(0)\left(1 - e^{-\frac{t}{\tau_p}}\right)} \quad (39a)$$

Case-II: After removal of illumination

After removal of illumination the optical generation rate (gop) becomes zero. However, the holes are still generated continuously due to thermal generation and disappear due to recombination. The net increase of hole concentration per second can be given by,

$$\frac{dp}{dt} = g_o - R = g_o - \frac{p}{\tau_p} \quad (40)$$

Where, g_o is increase in hole concentration per second due to thermal agitation, p/τ_p is rate of decrease in hole concentration due to recombination and τ_p is average life time of holes.

At steady state after removal of illumination, dp/dt = 0 and the hole concentration reaches the thermal equilibrium level of p_o.

$$\Rightarrow \quad g_o - \frac{p_o}{\tau_p} = 0$$

$$\Rightarrow \quad g_o = \frac{p_o}{\tau_p} \quad (41)$$

Putting above relation in equation (40), we have,

$$\frac{dp}{dt} = \frac{p_o - p}{\tau_p} = -\frac{p - p_o}{\tau_p} = -\frac{\delta p}{\tau_p}$$

where, $\delta p = p - p_o =$ Excess minority carrier concentration

Differentiating above equation w.r.t. time, we have,

$$\Rightarrow \quad \frac{d(\delta p)}{dt} = \frac{d(p - p_o)}{dt} = \frac{dp}{dt}$$

$$\Rightarrow \quad \frac{d(\delta p)}{dt} = -\frac{\delta p}{\tau_p} \quad (42)$$

The solution of above differential equation can be given as,

$$\Rightarrow \quad \boxed{\delta p(t) = \delta p(0) e^{-\frac{t}{\tau_p}}} \quad (43)$$

Example 10

An *n*-type silicon sample is uniformly illuminated with light which generates 10^{20} electron-hole

pairs per cm^3 per second. The minority carrier lifetime in the sample is 1 μs. In the steady state, the hole concentration in the sample is approximately 10^x, where x is an integer. The value of x is

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Solution : Ans. : 14

The excess minority carrier generation under uniform illumination of n-type sample is given by,

$$\delta p = g_{op}\tau_p$$

Where g_{op} is called optical generation rate and is average life time of minority carriers.

Given, $g_{op} = 10^{20}$ holes per cm^3 per second

And $\tau_p = 1\ \mu s$

$\Rightarrow$ $\delta p = 10^{20} \times 10^{-6} = 10^{14}$

The hole concentration in the sample is given by,

$$p = \delta p + p_o$$

Where p_o is concentration of minority carriers under steady state when no illumination is applied. When sample is illuminated,

$$\delta p >> p_o$$

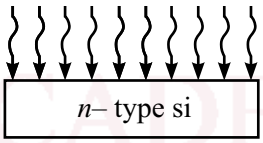
$\therefore$ $p \approx \delta p$

$\Rightarrow$ $p = 10^{14} = 10^x$

Where, $x = 14$

Example 11

Consider a silicon sample at T = 300 K, with a uniform donor density $N_d = 5 \times 10^{16}\ cm^{-3}$ illuminated uniformly such that the optical generation rate is $G_{opt} = 1.5 \times 10^{20}\ cm^{-3}\ s^{-1}$ throughout the sample. The incident radiation is turned off at $t = 0$. Assume low-level injection to be valid and ignore surface effects. The carrier lifetimes are $\tau_{po} = 0.1\ \mu s$ and $\tau_{no} = 0.5\ \mu s$.



The hole concentration at $t = 0$ and the hole concentration at $t = 0.3\ \mu s$, respectively, are

(a) $1.5 \times 10^{13}\ cm^{-3}$ and $7.47 \times 10^{11}\ cm^{-3}$ (b) $1.5 \times 10^{13}\ cm^{-3}$ and $8.23 \times 10^{11}\ cm^{-3}$

(c) $7.5 \times 10^{13}\ cm^{-3}$ and $3.73 \times 10^{11}\ cm^{-3}$ (d) $7.5 \times 10^{13}\ cm^{-3}$ and $4.12 \times 10^{11}\ cm^{-3}$

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Solution : Ans.(a)

The excess minority carrier generation under uniform illumination of n-type sample is given by,

$$\delta p = g_{op}\tau_p$$

Where g_{op} is called optical generation rate and τ_p is average life time of minority carriers.

Given, $g_{op} = 1.5 \times 10^{20}\ cm^{-3}\ s^{-1}$

And $\tau_p = 0.1\ \mu s$

$$\Rightarrow \qquad \delta p = 1.5 \times 10^{20} \times 0.1 \times 10^{-6} = 1.5 \times 10^{13}$$

The hole concentration in the sample is given by,

$$\Rightarrow \qquad p = \delta p + p_o$$

Where p_o is concentration of minority carriers under steady state when no illumination is applied. When sample is illuminated,

$$\delta p >> p_o$$

$$\therefore \qquad p \approx \delta p$$

$$\Rightarrow \qquad p = 1.5 \times 10^{13}\ \text{cm}^{-3}$$

If incident radiation is turned off at t = 0, the concentration of holes a t = 0,

$$p(0) = 1.5 \times 10^{13}\ \text{cm}^{-3}$$

The variation in concentration of excess holes for t > 0 after removal of illumination is given by,

$$\delta p(t) = \delta p(0)\, e^{-\frac{t}{\tau_p}}$$

Here, $\delta p(0) \approx p(0) = 1.5 \times 10^{13}\ \text{cm}^{-3}$

The hole concentration at $t = 0.3\ \mu s$

$$\Rightarrow \qquad \delta p(t) = 1.5 \times 10^{13}\, e^{-\frac{0.3}{0.1}} = 1.5 \times 10^{13}\, e^{-3}$$

$$\Rightarrow \qquad \delta p(t) = 7.47 \times 10^{11}\ \text{cm}^{-3}$$

$$\therefore \qquad p(t) \approx \delta p(t) = 7.47 \times 10^{11}\ \text{cm}^{-3}$$

1.14 Continuity Equation

The continuity equation gives the rate of change of carrier concentration inside a differential section of semiconductor bar. It can be derived on the concept that charge can neither be created nor be destroyed.

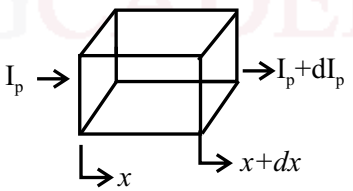

Fig. 12 Conservation of charge and continuity equation

Consider a differential volume of semiconductor bar with length dx and cross-section A. Le the hole current entering into the bar is I_p and hole current leaving the bar is $I_p + dI_p$. The additional current generated in the volume dI_p results in flow of additional holes front he differential volume. Therefore, the hole concentration reduces inside the volume due to outward flow of holes. If q is charge of hole then the decrease in number holes per second in the volume is equal to dI_p/q. The decrease in number

of holes per unit volume per second can be given by,

$$\frac{1}{Adx}\frac{dI_p}{q} = \frac{1}{q}\frac{\partial(I_p / A)}{\partial x} = \frac{1}{q}\frac{\partial J_p}{\partial x} \quad (44)$$

Where, J_p is holes current density inside bar.
Increase in hole concentration per unit time due to thermal generation,

$$g = \frac{p_o}{\tau_p}$$

Where τ_p is average life time of holes.

The decrease in hole concentration per unit time due to recombination $= \frac{p}{\tau_p}$

The total change of concentration of holes as a function of time is given by,

$$\frac{\partial p}{\partial t} = \frac{p_0 - p}{\tau_p} - \frac{1}{q}\frac{\partial J_p}{\partial x} \quad (45)$$

Above equation is known as continuity equation. In the continuity equation, $\frac{p_0 - p}{\tau_p}$ indicates change in concentration due to generation and recombination and $-\frac{1}{q}\frac{\partial J_p}{\partial x}$ indicates decrease in concentration due to drift current, J_p .

Note : *The continuity equation obeys the law of conservation of charge.*

1.15 Diffusion

Diffusion is a process of shifting of charge carriers from higher concentration to lower concentration. Diffusion is also a natural process. The minority carrier injection also results in diffusion of minority carrier from the point of injection towards region of lower concentration. Consider a n-type semiconductor bar is illuminated at one end with a light of suitable wavelength. The excess charge carriers generated at point of illumination start diffusing towards the region of lower concentration at another end. The concentration of charge carriers varies exponentially as a function of distance due to diffusion as shown in Fig.13. Let concentration of excess minority carriers i.e. holes is much smaller than the concentration of electrons. Such condition is called low level injection.

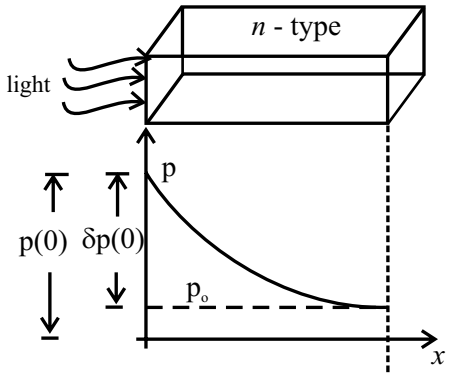

Fig. 13 Minority carrier injection and diffusion

When bar is illuminated, the concentration level of holes at the point of illumination becomes high. The percentage change in concentration of minority carrier holes due to illumination is very high as compare to majority carriers. The diffusion current due to holes is given by,

$$J_{p,\,diff} = -q\,D_p\frac{dp}{dx} \tag{46}$$

As per continuity equation, the rate of change of concentration of holes per unit second inside the bar will be,

$$\frac{\partial p}{\partial t} = \frac{p_0 - p}{\tau_p} - \frac{1}{q}\frac{\partial J_p}{\partial x} \tag{47}$$

$$\Rightarrow \quad \frac{\partial p}{\partial t} = \frac{p_0 - p}{\tau_p} - \frac{1}{q}\frac{\partial}{\partial x}\left(-q\,D_p\frac{dp}{dx}\right)$$

Under steady state, $\frac{\partial p}{\partial t} = 0$

$$\Rightarrow \quad \frac{p_0 - p}{\tau_p} - \frac{1}{q}\frac{\partial}{\partial x}\left(-q\,D_p\frac{dp}{dx}\right) = 0$$

$$\Rightarrow \quad \frac{d^2p}{dx^2} = \frac{p - p_0}{D_p\tau_p} = \frac{p - p_0}{L_p^{\,2}} \tag{48}$$

Where $L_p = \sqrt{D_p\,\tau_p}$ (49)

Here L_p is called diffusion length of holes and τ_p is average life time of holes. The diffusion length is average distance traveled by hole before recombination occurs.

The excess minority carriers concentration,

$$\delta p = p - p_o \tag{50}$$

$$\Rightarrow \quad p = \delta p + p_o$$

Differentiating twice w.r.t x, we have,

$$\frac{d^2p}{dx^2} = \frac{d^2(\delta p)}{dx^2} \tag{51}$$

$$\Rightarrow \quad \frac{d^2(\delta p)}{dx^2} = \frac{\delta p}{L_p^{\,2}} \tag{52}$$

The solution of above differential equation is given by,

$$\delta p(x) = K_1 e^{-\frac{x}{L_p}} + K_2 e^{+\frac{x}{L_p}} \quad (53)$$

The concentration decreases in +x direction. Therefore, $K_2 = 0$

At x = 0, $\delta p = \delta p(0) = p(0) - p_o$

$\Rightarrow$ $K_1 = \delta p(0) = p(0) - p_o$

$\Rightarrow$ $$\boxed{\delta p(x) = \delta p(0) e^{-\frac{x}{L_p}}} \quad (54)$$

$\Rightarrow$ $p - p_o = (p(0) - p_o)\, e^{-\frac{x}{L_p}}$

$\Rightarrow$ $$p = p_0 - (p_0 - p(0))\, e^{-\frac{x}{L_p}} \quad (55)$$

Where D_p is called diffusion constant of holes and τ_p is average life time of holes

Similarly, the diffusion length of electrons is given by,

$\Rightarrow$ $$L_n = \sqrt{D_n \tau_n} \quad (56)$$

Where D_n is called diffusion constant of electrons and τ_n is average life time of electrons.

1.16 Einstein Relation

It gives the relation between diffusion constant and mobility of charge carriers. The Einstein relation is defined by,

$$\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = V_T = \frac{kT}{q} = \frac{T}{11600} \quad (57)$$

Where, V_T is called *thermal voltage*. At room temperature, V_T = 26 mV.

Example 12

At T = 300 K, the hole mobility of a semiconductor μ_p = 500 cm²/V-s and kT/q = 26 mV. The hole diffusion constant D_p in cm²/s is_____

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Solution:Ans (12.9 to 13.1)

Given, μ_p = 500 cm²/V-s and kT/q = 26 mV

According to Einstein relationship,

$$\frac{D_p}{\mu_p} = \frac{kT}{q}$$

$\Rightarrow$ $$D_p = \frac{kT}{q} \times \mu_p$$

$$\Rightarrow \quad D_p = 26 \times 10^{-3} \times 500 = 13 \text{ cm}^2/\text{s}$$

1.17 Components of Current in Semiconductors

The current in semiconductors has two components called drift and diffusion currents. The drift current exists due to potential gradient applied across the semiconductor. The potential gradient applied across the semiconductors causes drifting of charge carriers resulting into drift current. The diffusion current exists due to concentration gradient inside the semiconductor. The concentration gradient causes natural diffusion of carriers from higher concentration to lower concentration resulting into diffusion current.

1.17.1 Drift Current

The drift current density inside the semiconductors is given by ,

$$J_{drift} = \sigma E \tag{58}$$

Where, σ is conductivity of semiconductor and E is electric field.

$$\Rightarrow \quad J_{drift} = e[n\mu_n + p\mu_p]E \tag{59}$$

$$J_{drift} = en\mu_n E + ep\mu_p E$$

$$J_{drift} = J_{n,drift} + J_{p,drift}$$

where, $J_{n,drift}$ is drift current of electrons and $J_{p,drift}$ is drift current of holes

$$\Rightarrow \quad J_{n,drift} = en\mu_n E \tag{60}$$

And $$J_{p,drift} = ep\mu_p E \tag{61}$$

1.17.2 Diffusion current

Diffusion current due to electrons is given by,

$$J_{n,diff} = e D_n \frac{dn}{dx} \tag{62}$$

Where D_n called is diffusion constant of electrons.
Similarly diffusion current of holes is given by,

$$J_{p,diff} = -e D_p \frac{dp}{dx} \tag{63}$$

Where D_p called is diffusion constant of holes. Negative sign indicates the current flows in the direction of decrease in concentration of holes or in the direction of negative concentration gradient of holes.

1.17.3 Total Current

Total current of electrons can be given by,

$$J_n = J_{n,drift} + J_{n,diff}$$

$$\Rightarrow \quad J_n = en\mu_n E + e D_n \frac{dn}{dx} \tag{64}$$

Total current of holes can be given by,

$$J_p = J_{p\,drift} + J_{p\,diff}$$

$$J_p = ep\mu_p E - eD_p \frac{dp}{dx} \quad (65)$$

1.17.4 Relationship between diffusion current of electrons and holes

For electrical neutrality in a semiconductor the excess carriers due to generation of electron-hole pairs is same for low level injection.

$$\therefore \quad n - n_o = p - p_o \quad (66)$$

$$\Rightarrow \quad \frac{dn}{dx} = \frac{dp}{dx} \quad (67)$$

The diffusion current of electron can be written as,

$$J_{n,diff} = qD_n \frac{dn}{dx} = qD_n \frac{dp}{dx} \quad (68)$$

$$\Rightarrow \quad J_{n,diff} = qD_n \frac{dn}{dx} = -\frac{D_n}{D_p}\left(-qD_p \frac{dp}{dx}\right) \quad (69)$$

$$\Rightarrow \quad \boxed{J_{n,diff} = -\frac{D_n}{D_o} J_{p,diff}} \quad (70)$$

1.17.5 Drift current of electrons and holes in terms of diffusion current of holes

$$J_{n,\,drift} = \left(\frac{D_n}{D_p} - 1\right) J_{p,diff} \quad (71)$$

$$J_{p,\,drift} = \frac{p}{n}\frac{\mu_p}{\mu_n}\left(\frac{D_n}{D_p} - 1\right) J_{p,diff} \quad (72)$$

1.17.6 Diffusion Current of Injected Minority Carriers in Semiconductors

When holes as minority carriers are injected into an n-type semiconductor the concentration of holes in the semiconductor is given by,

$$p = p_0 - (p_0 - p(0))\, e^{-\frac{x}{L_p}} \quad (73)$$

$$\frac{dp}{dx} = -\frac{(p(0) - p_0)}{L_p} e^{-\frac{x}{L_p}}$$

The diffusion current density of holes,

$$J_{p,diff} = -qD_p \frac{dp}{dx} = \frac{qD_{p0}(p(0) - p_0)}{L_p} e^{-\frac{x}{L_p}} \quad (74)$$

Diffusion current of holes,

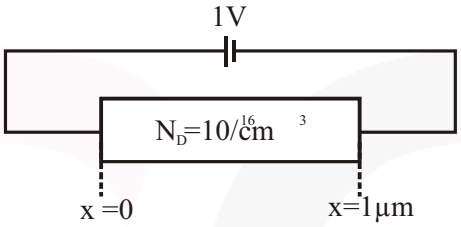
$$I_{p,diff} = AJ_{p,diff}$$

$$\boxed{I_{p,diff} = \frac{AqD_{p0}(p(0) - p_0)}{L_p} e^{-\frac{x}{L_p}}} \quad (75)$$

Example 13

Statement for Linked Answer questions 30 and 31 :

The silicon sample with unit cross -sectional area shown below is in thermal equilibrium. The following information is given : T = 300 K, electronic charge = 1.6×10^{-19} C, thermal voltage = 26 mV and electron mobility = 1350 cm^2/V-s.



(i) The magnitude of the electric field at x = 0.5 μm is

(a) 1 kV/cm (b) 5 kV/cm

(c) 10 kV/cm (d) 26 kV/cm

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(ii) The magnitude of the electron drift current density at x = 0.5 μm is

(a) 2.16×10^4 A/cm^2 (b) 1.08×10^4 A/cm^2

(c) 4.32×10^3 A/cm^2 (d) 6.48×10^2 A/cm^2

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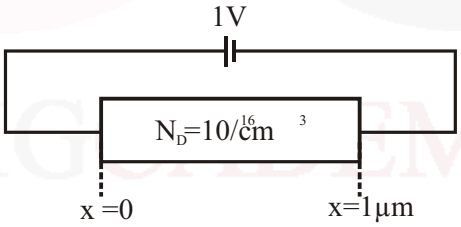
(i) Solution : Ans.(c)



Electric field inside the semiconductor will be uniform throughout the sample and can be given by

$$E = \frac{V}{L} = \frac{1}{1 \times 10^{-6}} V/m$$

$$\Rightarrow \quad E = 10 \text{ kV/cm}$$

(ii) Solution : Ans.(a)

The drift current density inside a uniformly doped semiconductor is given by,

$$J = \sigma E$$

Where, $\sigma = q(n\mu_n + p\mu_p)$

For n-type semiconductor bar,

$$\sigma = q N_D \mu_n$$

$$\Rightarrow \quad \sigma = 1.6 \times 10^{-19} \times 10^{16} \times 1350 = 2.16 \text{ mho-cm}^{-1}$$

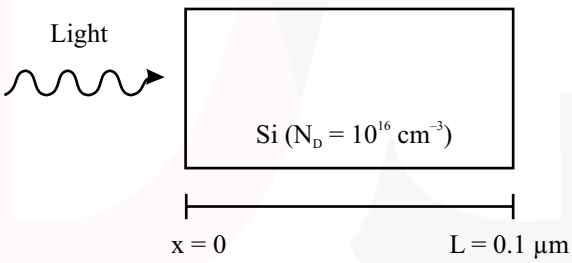
Electric field intensity inside the bar is uniform throughout the length of bar.

$$\therefore \quad E = 10 \text{ kV/cm} ; \text{ at } x = 0.5 \ \mu\text{m}.$$

$$\Rightarrow \quad J = \sigma E = 2.16 \times 10^4 \text{ A/cm}^2$$

Example 14

As shown a uniformly doped Silicon (Si) bar of length L = 0.1 μm with a donor concentration $N_D = 10^{16}$ cm^{-3} is illuminated at x = 0 such that electron and hole pairs are generated at the rate of $G_L = G_{L0}\left(1-\frac{x}{L}\right), 0 \le x \le L$, where $G_{L0} = 10^{17}$ cm^{-3} s^{-1}. Hole lifetime is 10^{-4} s, electronic charge q = 1.6×10^{-19} C, hole diffusion coefficient $D_p = 100$ cm^2/s and low level injection condition prevails. Assuming a linearly decaying steady state excess hole concentration that goes to 0 at x = L, the magnitude of the diffusion current density at x = L/2, in A/cm2, is _____.



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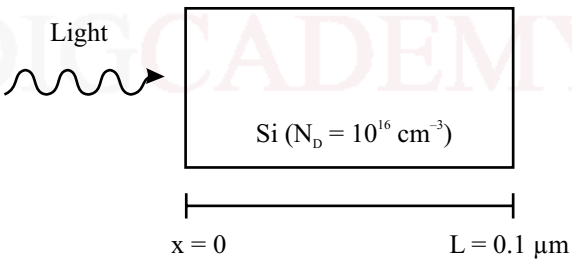
Solution : Ans.(15.9 to 16.1)



The rate of generation of holes due to illumination of n-type semiconductor can be given,

$$g = \frac{p}{\tau_p}$$

Given, $g = G_L = G_{LO}\left(1-\frac{x}{L}\right)$

$$\Rightarrow \qquad p = g\tau_p = G_{LO}\tau_p\left(1-\frac{x}{L}\right)$$

Concentration gradient of holes across length of the bar,

$$\frac{dp}{dx} = -\frac{G_{LO}\tau_p}{L}$$

The diffusion current of holes is given by,

$$J_p = -q D_p \frac{dp}{dx}$$

$$\Rightarrow \qquad J_p = -q D_p\left(-\frac{G_{LO}\tau_p}{L}\right) = \frac{q D_p G_{LO}\tau_p}{L}$$

Given. $G_{Lo} = 10^{17}\ cm^{-3}\ s^{-1}$, $\tau_p = 10^{-4}$ s, $L = 0.1\ \mu m = 10^{-5}$ cm , $D_p = 100\ cm^2/s$ and $q = 1.6 \times 10^{-19}$ C

$$\therefore \qquad J_p = \frac{1.6\times10^{-19}\times100\times10^{17}\times10^{-4}}{10^{-5}} = 16\ A/cm^2$$

1.18 Induced Electric Field and Potential Variation in Graded Semiconductors

A semiconductor bar with varying amount of doping levels is called graded semiconductor. Consider a open circuited p-type semiconductor bar having concentration p_1 and p_2 at point x_1 and x_2 respectively.

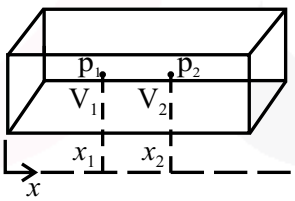


Fig. 14 Graded semiconductor

The concentration gradient in the bar shown above results in diffusion current. The total current inside open circuited bar is always zero. So, to counter balance the diffusion current a voltage is induced between x_1 and x_2 which causes an equal and opposite drift current. So net current inside the bar is zero.

$$I_{p,\,diff} + I_{p,\,drift} = 0 \qquad (76)$$

$$\Rightarrow \qquad -e D_p \frac{dp}{dx} + e\mu_p p E = 0$$

$$\Rightarrow \qquad E = \frac{1}{p}\left(\frac{D_p}{\mu_p}\right)\frac{dp}{dx} \qquad (77)$$

As per Einstein relation, $\frac{D_p}{\mu_p} = V_T$

The induced electric field in the semiconductor becomes,

$$\Rightarrow \quad \boxed{E = \frac{V_T}{p}\frac{dp}{dx}} \tag{78}$$

but $$E = -\frac{dV}{dx} \tag{79}$$

$$\Rightarrow \quad -\frac{dV}{dx} = \frac{V_T}{p}.\frac{dp}{dx}$$

$$\Rightarrow \quad dV = -V_T\frac{dp}{p}$$

$$\int_{V_1}^{V_2} dV = -V_T\int_{p_1}^{p_2}\frac{dp}{p}$$

Integrating both side, we have,

$$\Rightarrow \quad V_2 - V_1 = -V_T\,[\ell n\, p]_{p_1}^{p_2}$$

$$\Rightarrow \quad V_2 - V_1 = V_{21} = -V_T\,\ell n\frac{p_2}{p_1}$$

$$\Rightarrow \quad \boxed{V_{21} = V_T\ell n\frac{p_1}{p_2}} \tag{80}$$

1.18.1 Induced Electric Field and Variation of potential in step graded pn semiconductor junction

Consider an abrupt semiconductor pn junction as shown in Fig.15. Let p_{po} is concentration of holes on *p*-side of junction and p_{no} is concentration of holes on n-side of the junction.

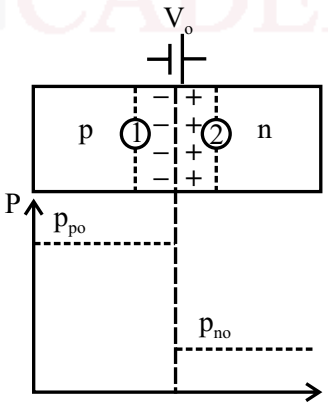


Fig. 15 Step graded semiconductor & induced electric field

The potential barrier across the junction can be given by using equation (80) as under,

$$V_o = V_n - V_p = V_T \ell n\left[\frac{p_{po}}{p_{no}}\right] \tag{81}$$

In p-type semiconductor, $p_{po} \approx N_A$ and according to law of mass action, $p_{no} \approx \frac{n_i^2}{N_D}$. Then the potential barrier across the junction becomes,

$$\Rightarrow \quad V_o = V_T \ell n\left(\frac{N_A}{n_i^2 / N_D}\right)$$

$$\Rightarrow \quad \boxed{V_o = V_T \ell n\left(\frac{N_A N_D}{n_i^2}\right)} \tag{82}$$

1.19. Fermi Level in Semiconductors

1.19.1 Fermi-Dirac Function

A Fermi-Dirac function represents the probability of occupying a quantum of energy E by an electron. Fermi-Dirac function is function of temperature and mathematically it is defined by

$$f(E) = \frac{1}{1 + e^{\frac{(E - E_F)}{kT}}} \tag{83}$$

Where E_F is called Fermi energy level, k is Boltzmann's constant, T is temperature in kelvin,

At $\quad E = E_F ; f(E) = \frac{1}{2}$

Thus, the Fermi level is an energy level with 50% probability of being filled if no forbidden band exists. The Fermi-Dirac function for metals as function of energy level and temperature is drawn as under,

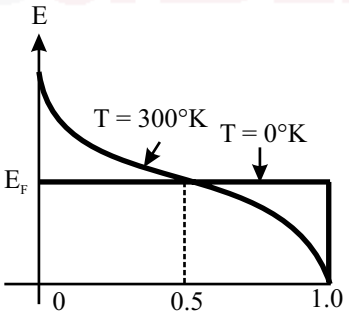


Fig. 16 Fermi Dirac function in metals

1.19.2 Density of States and Fermi-level in metals

Fermi level in metals can be obtain on assumption that all the energy levels below Fermi level are filled with electrons and all the energy levels above Fermi level are empty. Such state of metal is called Degenerate. The electrons density in metals can be given by,

$$dn = \rho_E \, dE \tag{84}$$

Where, ρ_E is the effective distribution of energy inside a metals in terms of number of electrons per electron-volt per cubic meter in metals. Mathematical it is given by,

$$\rho_E = f(E)\, N(E)$$

Here, N(E) represents possible density of states expressed in terms of electrons per electron-volt per cubic meter.

The density of states N(E) is related to Energy E is as under,

$$N(E) = \gamma E^{1/2} \tag{85}$$

Where, $\gamma = \frac{4\pi}{h^3}(2m)^{3/2}(1.6\times10^{-19})^{3/2} = 6.82\times10^{27}$

Under degenerate mode all the energy levels below E_F are occupied by electrons so probability of finding the electron below Fermi level, f(E) = 1.

$$\therefore \quad \rho_E = N(E) = \gamma E^{1/2} \; ; E < E_F \tag{86}$$

$$\Rightarrow \quad n = \int_0^{E_F} \gamma E^{1/2} dE = \gamma \frac{E^{3/2}}{3/2}\Big|_0^{E_F}$$

$$\Rightarrow \quad n = \frac{2}{3}\gamma E_F^{3/2}$$

$$\Rightarrow \quad E_F = \left(\frac{3n}{2\gamma}\right)^{2/3} \tag{87}$$

Note : *At 0 °K, the electrons have energy extending from 0 to E_F in order to satisfy the Pauli's exclusion principle. So, not all electrons have same energy at 0 °K.*

1.19.3 Concentration of Electrons and Holes in Semiconductors

The concentration of free electrons per cubic meter in conduction band whose energies lie between E and E+dE in the conduction band is given by,

$$dn = \rho_E dE$$

Where, ρ_E is the energy distribution inside the conduction band in terms of number of electrons per electron-volt per cubic meter.

The function ρ_E is given by,

$$\rho_E = f(E)\, N(E)$$

The possible density of states for electrons in conduction band is given by,

$$N(E) = \gamma(E - E_c)^{1/2} \text{ for } E > E_c \quad (88)$$

The Fermi -Dirac function is given by,

$$f(E) = \frac{1}{1+e^{(E-E_F)/kT}}$$

For $E > E_c$, $E - F_F >> kT$, then

$$f(E) \approx e^{-(E-E_F/kT} \quad (89)$$

Then concentration of electronics in conduction band becomes,

$$dn = \rho_E dE = f(E)N(E)dE \quad (90)$$

$$\Rightarrow \quad dn = \gamma(E - E_c)^{1/2} e^{(E-E_F)kT} dE$$

Integrating above equation by taking limits of E varies from E_c to ∞

$$\therefore \quad n = \int_{E_c}^{\infty} \gamma\left(E - E_c\right)^{1/2} e^{-(E-E_F)kT} dE$$

Above integration gives, $n = N_C\, e^{-(E_C - E_F)/kT}$ (91)

where, $N_c = 2\left(\frac{2\pi m_n k\,T}{h^2}\right)^{\frac{3}{2}}$ = Density of states in conduction band

Here, k is Boltzmann constant in Joules/°K and m_n is effective mass of electron.

The density of states for holes in valence band is given by,

$$N(E) = r(E - E_c)^{1/2} \text{ for } E > E_c \quad (92)$$

The Fermi-Dirac function for hole is 1 – f(E) where f(E) is probability that the energy level E is occupied by an electron.

$$1 - f(E) = \frac{1}{1+e^{(E-E_F)kT}} = \frac{e^{(E-E_F)kT}}{1+e^{(E-E_F)kT}} = \frac{e^{-(E_F-E)kT}}{1+e^{-(E_F-E)kT}} \quad (93)$$

For valence band, $E_F - E >> kT$, so $e^{-(E_F-E)kT} \approx 0$

$$\Rightarrow \quad 1 - f(E) \approx e^{-(E_F-E)kT} \quad (94)$$

The holes per cubic meter in valence band between energy level E to E + dE can be given by,

$$dp = (1-f(E))\, N(E)\, dE \quad (95)$$

For valence band, $E_v < E < -\infty$

$$\Rightarrow \qquad p = \int_{-\infty}^{E_v} \gamma\left(E_v - E\right)^{1/2} e^{-(E_F - E)/kT} dE$$

Above integration gives, $p = N_v e^{-(E_F - E_v)/kT}$ (96)

Where, $N_v = \left(\frac{2\pi m_p kT}{h^2}\right)^{3/2}$ = The density of states in valence band where m_p is effectives mass of hole.

From the equations (91) and (96), we have,

$$np = \left(N_C e^{-(E_C - E_F)/kT}\right)\left(N_v e^{-(E_F - E_v)/kT}\right)$$

$$\Rightarrow \qquad np = N_C N_v e^{-(E_C - E_V)/kT} = N_C N_v e^{-E_g/kT}$$

As per law of mass action, $np = n_i^2$ (97)

$$\Rightarrow \qquad n_i^2 = N_C N_v e^{-E_g/kT}$$

$$\Rightarrow \qquad n_i = \sqrt{N_C N_v}\, e^{-E_g/2kT} \qquad (98)$$

The Fermi level in intrinsic semiconductors, the Fermi-Dirac probability function at 0°K and 300°K, the density of states in each band and density of energies ρ_E for electrons and holes can be drawn as under,

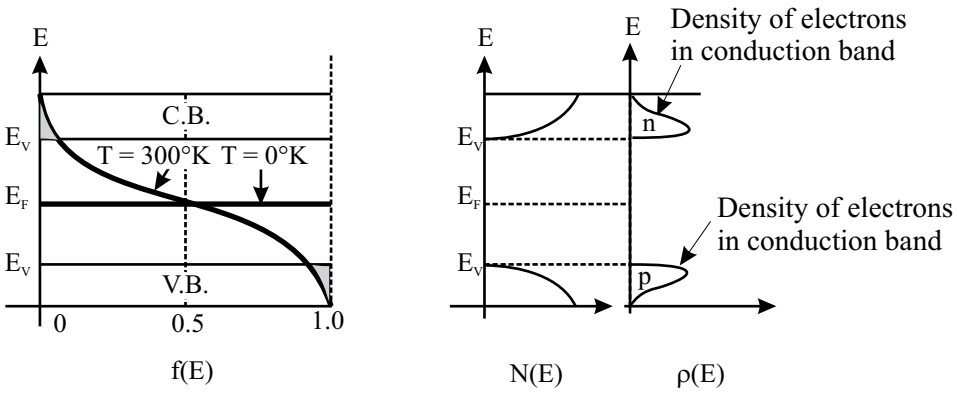


Fig. 17 Fermi Dirac function, density of state and density of electrons in semiconductors.

1.19.4 Fermi Level in Intrinsic Semiconductor

For intrinsic semiconductors, $n = p = n_i$ (99)

$$\Rightarrow \qquad N_C e^{-\frac{(E_C - E_F)}{kT}} = N_V e^{-\frac{(E_F - E_V)}{kT}}$$

$$\Rightarrow \quad \frac{N_C}{N_V} = e^{(E_V + E_C - 2E_F)/kT}$$

$$\Rightarrow \quad ln\frac{N_C}{N_V} = \frac{E_C + E_V - 2E_F}{kT}$$

$$\Rightarrow \quad E_C + E_V - 2E_F = kT\, ln\frac{N_C}{N_V}$$

$$\Rightarrow \quad E_F = \frac{E_C + E_V}{2} + \frac{kT}{2} ln\frac{N_V}{N_C} = E_{Fm} + 0.5\ kT\, ln\frac{N_C}{N_V} \qquad .(100)$$

Where E_{Fm} is mid band Fermi level.

If effective mass of electron is equal to the effective mass of hole then $N_V = N_C$.

$$\Rightarrow \quad E_F = E_{Fm} = \frac{E_C + E_V}{2} \qquad (101)$$

Thus Fermi level in intrinsic semiconductors lies at the middle of energy gap as shown if the figure below.

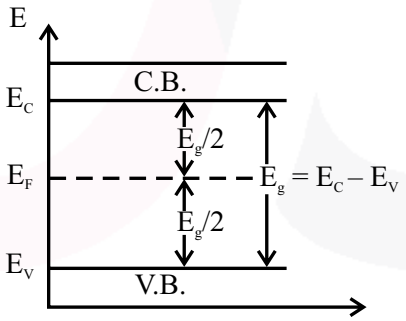


Fig. 18 Fermi level in intrinsic semiconductors.

Where, E_C is lowest energy level of conduction band(C.B.) , E_V is highest energy level of valence band (V. B.) and E_F is Fermi level.

$$E_F = E_V + \frac{E_g}{2} = E_C - \frac{E_g}{2} \qquad (102)$$

Note : *The Fermi level in intrinsic semiconductor is always at the center of energy gap irrespective of the temperature of the semiconductor.*

1.19.5 Fermi Level in n-type Semiconductor

In n-type semiconductors the density of occupied energy states by electrons is more in conduction band than concentration of holes in valence band so the Fermi level (E_F) lies close due conduction band as shown in Fig.19. However, intrinsic Fermi level (E_{Fi}) lies at the center of energy gap.

The concentration of electrons in extrinsic *n*-type semiconductors is given by

$$n = N_C e^{-\frac{(E_C - E_F)}{kT}} \quad (103)$$

For n-type semiconductors, $n \approx N_D$

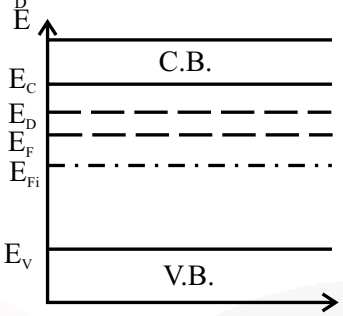


Fig. 19 Fermi level in n-type semiconductors.

$$\Rightarrow \quad N_D = N_C e^{-\frac{(E_C - E_F)}{kT}} \quad (104)$$

$$\Rightarrow \quad -E_C + E_F = kT \ln\left[\frac{N_D}{N_C}\right]$$

$$\Rightarrow \quad E_F = E_C - kT \ln\frac{N_C}{N_D} \quad (105)$$

Effect of Temperature on Fermi level:

From the above equation it is clear Fermi level shifts downward (i.e. towards center of energy gap) with increase in temperature. But Fermi level always lies in the upper half of energy gap because the occupied energy states by electrons in conduction band are always more than concentration of holes in n-type semiconductors.

Effect of Donor concentration :

As donor concentration is increased the density of occupied energy states, by electrons of donor impurity in conduction band, is increased and hence the Fermi level is also increased. Mathematically, the Fermi level increases with increase in donor concentration. The Fermi level shifts with respect to donor concentration as follows,

Case-I : If $N_D < N_C$ then $E_F < E_C$

Case-II : If $N_D = N_C$ then $E_F = E_C$

Case-III : If $N_D > N_C$ then $E_F > E_C$

Thus, when donor concentration is very high such that $N_D > N_C$, the Fermi level can shift in conduction band.

Note : *Fermi level on n-side of Tunnel diode lies in the conduction due to its heavy doping level on n-side of diode.*

Shift of Fermi Level(E_F) from intrinsic level (E_{Fi}):

The shift of Fermi level (E_F) from the intrinsic level(E_{Fi}) can be obtained by using the following relation,

$$n = N_C e^{-\frac{(E_C - E_F)}{kT}} = N_C e^{-\frac{(E_C - E_{Fi}) - (E_F - E_{Fi})}{kT}} \quad (106)$$

$$\Rightarrow \quad n = N_C e^{-\frac{(E_C - E_{Fi})}{kT}} \times e^{\frac{(E_F - E_{Fi})}{kT}}$$

$$\Rightarrow \quad \boxed{n = n_i e^{\frac{E_F - E_{Fi}}{kT}}} \quad (107)$$

where $n_i = N_C e^{-\frac{(E_C - E_{Fi})}{kT}}$ = concentration of electrons at intrinsic level

$$\Rightarrow \quad E_F - E_{Fi} = kT \, ln \, \frac{n}{n_i} \quad (108)$$

Note : *For n-type semiconductors 'n' can be replaced by N_D and compensated semiconductors 'n' can be replaced by $N_D - N_A$ in above equations.*

1.19.6 Fermi Level in p-type Semiconductor

In p-type semiconductors the density of occupied energy states by electrons is less in conduction band than the concentration of holes in valence band so the Fermi level (E_F) lies close due valence band in p-type semiconductors. However, intrinsic Fermi level (E_{Fi}) lies at the center of energy gap.

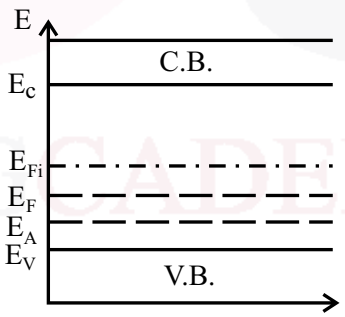


Fig. 20 Fermi level in p-type semiconductors.

The concentration of holes in extrinsic p-type semiconductors is given by

$$p = N_V e^{-\frac{(E_F - E_V)}{kT}}$$

For p-type semiconductors, $p \approx N_A$

$$\Rightarrow \quad N_A = N_V e^{-\frac{(E_F - E_V)}{kT}} \quad (109)$$

$$\Rightarrow \quad -E_F + E_V = kT \ln\left[\frac{N_A}{N_V}\right]$$

$$\Rightarrow \quad E_F = E_V + kT \ln\frac{N_V}{N_A} \qquad (110)$$

Effect of Temperature on Fermi-level

From the above equation it is clear Fermi level shifts upward (i.e. towards center of energy gap) with increase in temperature. But Fermi level always lies in the lower half of energy gap because the occupied energy states by electrons in conduction band are always less than concentration of holes in p-type semiconductors.

Effect of Acceptor concentration :

As acceptor concentration is increased the hole concentration in valence band increases and Fermi level shifts towards the valence band. Mathematically, the Fermi level decreases with increase in acceptor concentration. The Fermi level shifts with respect to acceptor concentration as follows,

Case-I : If $N_A < N_V$ then $E_F > E_V$

Case-II : If $N_A = N_V$ then $E_F = E_V$

Case-III : If $N_A > N_V$ then $E_F < E_V$

Thus, when acceptor concentration is very high such that $N_A > N_V$, the Fermi-level can shift in valence band.

Note : *Fermi level on p-side of Tunnel diode lies in the valence band due to its heavy doping level of diode on p-side.*

Shift of Fermi Level(E_F) from intrinsic level (E_{Fi}):

The shift of Fermi level (E_F) from the intrinsic level(E_{Fi}) can be obtained by using the following relation,

$$p = N_V e^{-\frac{(E_F - E_V)}{kT}} = N_V e^{-\frac{(E_{Fi} - E_V) - (E_{Fi} - E_F)}{kT}} \qquad (111)$$

$$\Rightarrow \quad p = N_V e^{-\frac{(E_{Fi} - E_V)}{kT}} \times e^{\frac{(E_{Fi} - E_F)}{kT}}$$

$$\Rightarrow \quad \boxed{p = n_i e^{\frac{E_{Fi} - E_F}{kT}}} \qquad (112)$$

where, $n_i = N_V e^{-\frac{(E_{Fi} - E_V)}{kT}}$ = concentration of electrons at intrinsic level

$$\Rightarrow \quad E_{Fi} - E_F = kT \ln \frac{p}{n_i} \qquad (113)$$

Note : *For p-type semiconductors 'p' can be replaced by N_A and compensated semiconductors 'p' can be replaced by $N_A - N_D$ in above equations.*

Example 15

Silicon is doped with boron to a concentration of 4×10^{17} atoms/cm^3. Assume the intrinsic carrier concentration of silicon to be 1.5×10^{10}/cm^3 and the value of $\frac{kT}{q}$ to be 25 mV at 300 K. Compared to undoped silicon, the Fermi level of doped silicon

(a) Goes down by 0.13 eV
(b) Goes up by 0.13 eV
(c) Goes down by 0.427 eV
(d) Goes up by 0.427 eV

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Solution : Ans.(c)

When p-type impurities (i.e. B, Al, Ga, In, Tn) are added to Si the Fermi level shifts down towards the valence band.

The concentration of holes in valence band p-type semiconductor is given by,

$$p = n_i e^{(E_{Fi}-E_F)/kT}$$

$$\Rightarrow \quad E_{Fi} - E_F = kT \ln \frac{p}{n_i}$$

Given, $\frac{kT}{q} = 25$ mV or $kT = 0.025$ eV, $n_i = 1.5\times10^{10}$ cm^{-3}

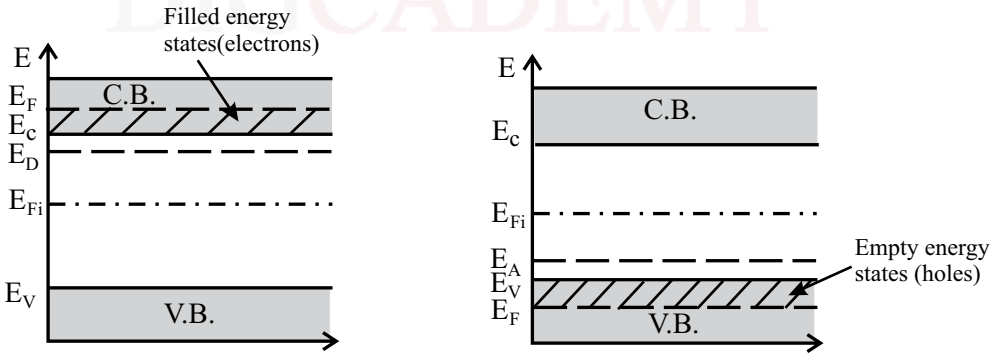
For given p-type material, $p \approx N_A = 4\times10^{17}$ cm^{-3}

$$\Rightarrow \quad E_{Fi} - E_F = 0.025 \ln \frac{4\times10^{17}}{1.5\times10^{10}} = 0.427 \text{ eV}$$

1.19.7 Non-degenerate Semiconductors and Degenerate Semiconductors

In normal level of doping of semiconductors the dopant are far apart and dopant introduce non-interacting energy states. Such type of semiconductors are called non-degenerate semiconductors.

When the concentration level of dopant is increased the energy level of dopant are no more discrete form bands of energies like conduction and valence bands of semiconductor atoms.



(a) Degenerate n-type semiconductor **(b) Degenerate p-type semiconductor**

Fig. 21 Fermi levels in n and p type semiconductors.

If the doping level of donor impurity atoms (N_D) in n-type semiconductors becomes more than the density of states in conduction band (N_C) then the Fermi level enters into the conduction band. This type of semiconductor is called n-type degenerate semiconductor. In degenerate n-type semiconductor the energy states above Fermi level are mostly empty and energy states between Fermi-level and lower level of conduction band (E_C) are mostly filled with electrons. So, concentration of electrons is high in conduction band.

If the doping level of acceptor impurity atoms (N_A) in p-type semiconductors becomes more than the density of states in valence band (N_V) then the Fermi level enters into the valence band. This type of semiconductor is called p-type degenerate semiconductor. In degenerate p-type semiconductor the energy states above Fermi level and upper level of valence band are mostly empty and energy states below Fermi-level are mostly filled with electrons. So, concentration of holes is high in valence band.

1.20 Hall's Effect

According to this effect if a specimen carrying a current is subjected to a transverse magnetic field, an electric field is induced in the direction perpendicular to both direction of current as well as magnetic field.

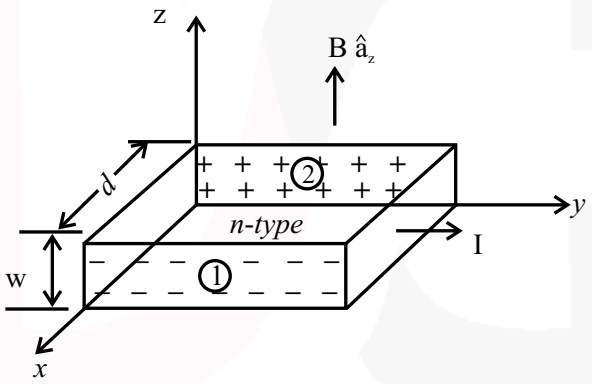


Fig. 22 Hall's effect in semiconductors.

Consider n-type semi-conducting bar carrying current in 'y' direction, with magnetic field applied in 'z' direction as shown in figure. The force experienced by a charge q in magnetic field is given by,

$$\vec{F}_B = q(\vec{v} \times \vec{B}) \qquad (114)$$

where v is drift velocity of charge carrier.

For electrons, $q = -e$, $v = -v_y \hat{a}_y$ and $\vec{B} = B\hat{a}_z$

$$\Rightarrow \quad \vec{F}_B = -e(-v_y B)(\hat{a}_y \times \hat{a}_z)$$

$$\vec{F}_B = ev_y B\hat{a}_x \qquad [\because \hat{a}_y \times \hat{a}_z = \hat{a}_x] \qquad (115)$$

Similarly for holes, $q = +e, v = +v_y \hat{a}_y$ and $\vec{B} = B\hat{a}_z$

$$\Rightarrow \quad \vec{F}_B = +e(v_y B)(\hat{a}_y \times \hat{a}_z)$$

$$\vec{F}_B = ev_y B\hat{a}_x \tag{116}$$

Thus, the force experienced by electrons and holes is in the same +x-direction. As the concentration of electrons is more in n-type semiconductor so the face 1 becomes negative and face 2 becomes positive. Because of accumulation of charges on faces 1 and 2 an electric field is induced in +x-direction inside the semiconductor bar. The induced electric field opposes further accumulation of electrons on the front face 1. If $E\hat{a}_x$ is the field induced in +x-direction then the force experienced by electron in –x-direction due to $E\hat{a}_x$ can be given by,

$$\vec{F}_E = -eE\hat{a}_x \tag{117}$$

At equilibrium, $|\vec{F}_E| = |\vec{F}_B|$

$$\Rightarrow \quad ev_y B = eE$$

$$\Rightarrow \quad E = v_y B \tag{118}$$

The potential difference between faces 1 and 2 of the bar due to the electric field E can be given by,

$$V_H = E\,d$$

This potential is known as Hall voltage.

$$\Rightarrow \quad V_H = v_y Bd$$

Relationship between drift velocity and conduction current density is given by,

$$J = \rho\, v_y \tag{119}$$

where, ρ charge density and v_y is drift velocity.

charge density, $\rho = en$ (120)

Then, $V_H = \frac{J}{\rho} Bd$

But, Current density, $J = \frac{I}{wd}$

$$\Rightarrow \quad V_H = \frac{BI}{\rho w} \tag{121}$$

Here 'w' is width in direction of $\vec{B}$.

Note : *If direction of either current or magnetic field is reversed the polarity of Hall voltage is reversed but if directions of both current and magnetic field are reversed, simultaneously, the polarity of Hall's voltage remains unchanged.*

Hall Coefficient **:** Hall's coefficient is defined as the inverse of charge density.

$$R_H = \frac{1}{\rho} \tag{122}$$

$$\Rightarrow \quad R_H = \frac{V_H w}{BI} \tag{123}$$

Hall co-efficient of semiconductors:

Case-I : Hall coefficient of n-type of semiconductors:

$$R_H = -\frac{1}{en} \tag{124}$$

where, n is concentration of electrons. Hall co-efficient is *negative* for n-type semiconductors.

Case-II : Hall coefficient of p-type of semiconductors:

$$R_H = \frac{1}{ep} \tag{125}$$

where, p is concentration of holes. Hall co-efficient is *positive* for p-type semiconductors.

Case-III : Hall coefficient for semiconductor with both types of impurities:

$$R_H = \frac{1}{e}\left(\frac{\mu_p^2 p - \mu_n^2 n}{(\mu_p p + \mu_n n)^2}\right) \tag{126}$$

For semiconductors with both types of impurities, R_H is negative if $\mu_p^2 p < \mu_n^2 n$ and it is positive if $\mu_n^2 n < \mu_p^2 p$.

Case-IV : Hall coefficient for intrinsic semiconductors :

For intrinsic semiconductor, $n = p = n_i$

$$R_H = -\frac{1}{en_i}\left(\frac{\mu_n^2 - \mu_p^2}{(\mu_n + \mu_p)^2}\right) \tag{127}$$

Since μ_n is more than μ_p, therefore, R_H is negative for intrinsic semiconductor.

Note : *The Hall voltage is zero for intrinsic semi conductors because the numbers of free electrons are equal to numbers of holes and both experienced force in same direction so the face 1 of semiconductor bar remains neutral.*

Note : *Hall effect is strongest in extrinsic semi conductors with single type of impurity and weakest in metals.*

Hall Angle :

Due to induced Hall voltage the resultant field is no longer longitudinal rather it makes an angle θ_H with field in y-direction. This angle is called Hall angle.

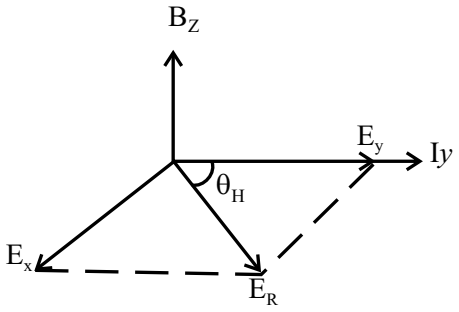


Fig. 23 Hall's angle.

The Hall angle is given by,

$$\tan \theta_H = \frac{E_x}{E_y} \tag{128}$$

The resultant field inside the semiconductor can be given by,

$$E_R = \sqrt{E_x^2 + E_y^2} \tag{129}$$

Applications of Hall effect :

i) It can be used for determination of type of semiconductor by seeing checking the polarity of faces.

ii) The charge carrier concentration can be determined by measuring the hall's co-efficient.

$$R_H = \frac{V_H w}{BI} = \frac{-1}{en} = +\frac{1}{ep}$$

iii) Mobility of charge carriers can be determined if conductivity is known

Conductivity of semiconductor, $\sigma = en(\mu_p + \mu_n)$

For n-type semiconductor, $\sigma \approx en\mu_n$,

$$\sigma = \frac{1}{R_H}.\mu_n$$

$$\Rightarrow \quad \mu_n = \sigma R_H \tag{130}$$

iv) Conductivity of semiconductor can be determined if mobility is known.

$$\sigma = \frac{1}{R_H}.\mu_n$$

v) Used as Hall effect multiplier.

vi) Used for measurement of magnetic flux using flux meter.

vii) Used in Poynting vector type wattmeter.

1.21 Photoconductor

Photoconductors the semiconductor devices which are used as photo-detectors for sensing the light.

These devices work on the principle of change in conductivity of semiconductors due th illumination. When a semiconducting material is illuminated with light of suitable wavelength there is breakage of covalent bond resulting in electron-hole pair generation When electron is moved from valence band to the conduction band the electron hole pair generation is intrinsic generation. The critical wavelength of light required for intrinsic excitation is given by,

$$\lambda_c = \frac{12400}{E_g} \overset{o}{A} \tag{131}$$

where E_g is band gap semiconductor in eV, λ_c is also called cut-off or threshold wavelength.

The most commonly used material for construction of photo-conductors is cadmium sulfide (CdS) because it has high dissipation, excellent sensitivity and low resistance, when stimulated by light. Other materials are lead sulfide(PbS) and selenium sulphide (SeS). The PbS detects the infrared and SeS detects the visible light.

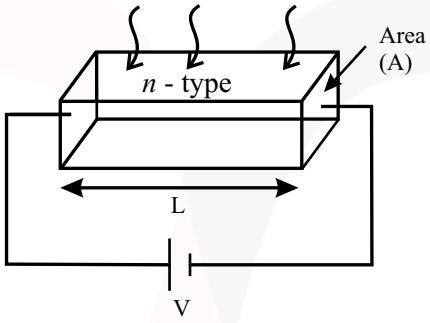


Fig. 24 Photo-conductor illuminated with light.

Consider a photo-conductor bar of length L which is connected to a voltage source V. Let it is illuminated with a light source. The conductivity of bar at thermal equilibrium will be,

$$\sigma_o = n_o e\mu_n + p_o e\mu_p \tag{132}$$

When semiconductor is illuminated let concentration of electrons changes from no to $n_o + \delta n$ and concentration of holes changes from po to $p_o + \delta p$. Whe δn and δp are excess electrons and holes generated due to illumination of the photoconductor.

Then conductivity of bar after illumination will be,

$$\sigma = (n_o + \delta n)e\mu_n + (p_o + \delta p)e\mu_p$$

$$\Rightarrow \quad \sigma = n_o e\mu_n + p_o e\mu_p + \delta n e\mu_n + \delta p e\mu_p = \sigma_o + \Delta\sigma$$

The change is conductivity due illumination,

$$\Delta\sigma = \delta n e\mu_n + \delta p e\mu_p \tag{133}$$

The g_{op} is optical generation rate of electron-hole pairs then the increase in concentration of electrons and holes is given by,

$$\delta p = g_{op}\tau_p \tag{134}$$

and

$$\delta n = g_{op}\tau_n \tag{135}$$

where, τ_p and τ_n are average life time of holes and electrons respectively. As semiconductor is electrically neutral so number of holes generated due to illumination are always equal to the number of electrons generated.

$$\delta p = \delta n$$

$$g_{op}\tau_p = g_{op}\tau_n$$

$$\Rightarrow \quad \tau_p = \tau_n \tag{136}$$

Then change in conductivity of the photoconductor becomes,

$$\Delta\sigma = eg_{op}\tau_p(\mu_n + \mu_p) \tag{137}$$

If E is electric field induced in the semiconductor due to applied voltage V then the current density in the semiconductor is,

$$J = J_o + J_{op} = (\sigma_o + \Delta\sigma)E \tag{138}$$

Where J_o is current density prior to optical illumination which is $\sigma_o E$ and J_{op} is optical current density which is $\Delta\sigma E$

The photo current in the photoconductor due to illumination can be given by,

Change is conductivity results in increase in current in semiconductor. The increased component of current is photo-current which is due to illumination of the photoconductor.

$$I_{op} = A\,J_{op} = A\Delta\sigma E = = Aeg_{op}E\tau_p(\mu_n + \mu_p) \tag{139}$$

Where A is area of the semiconductor bar or photoconductor.

The transit time of electron required for an electron to flow through the photoconductor is

$$t_n = \frac{L}{v_d} = \frac{L}{\mu_n E} \tag{140}$$

$$\Rightarrow \quad E = \frac{L}{\mu_n t_n} \tag{141}$$

Putting above expression of E in equation (1.107), we have,

$$I_{op} = \frac{ALeg_{op}\tau_p}{t_n}\left(1 + \frac{\mu_p}{\mu_n}\right) \tag{142}$$

Photoconductor gain:

Gain of photoconductor is defined as ratio of the rate at which charge is collected by the contacts to the rate at which charge is generated with volume of photoconductor. Mathematically,

$$\Gamma_{ph} = \frac{I_{op}}{eg_{op}AL} = \frac{\tau_p}{t_n}\left(1 + \frac{\mu_p}{\mu_n}\right) \tag{143}$$

Note : *The generation of holes in valance band due to shifting of electrons from valence band to acceptor level and generation of electrons due to shifting of electrons from donor level to conduction band is called extrinsic excitation. Since the density of states at donor and acceptor level are much lower than the density of states at conduction band and valance band so the photoconductity is principally due to intrinsic excitation.*

Example 16

The longest wavelength that can be absorbed by silicon, which has the bandgap of 1.12 eV, is 1.1mm. If the longest wavelength that can be absorbed by another material is 0.87 mm, then the bandgap of this material is

(a) 1.416 eV (b) 0.886 eV

(c) 0.854 eV (d) 0.706eV

GATE(EC/2004/2M)

Solution : Ans.(a)

Longest wavelength for intrinsic excitation,

$$\lambda_c = \frac{1.24}{E_g} \ \mu m$$

$$\Rightarrow \quad \lambda_c E_g = 1.24 = \text{constant}$$

$$\Rightarrow \quad \lambda_{c,Si} E_{g,Si} = \lambda_{c,X} E_{g,X}$$

$$\Rightarrow \quad E_{g,X} = \lambda_{c,Si} E_{g,Si} \ / \ \lambda_{c,X}$$

$$\Rightarrow \quad E_{g,X} = \frac{1.1 \times 1.12}{0.87} = 1.416 \text{eV}$$

Example 17

At T = 300 K, the band gap and the intrinsic carrier concentration of GaAs are 1.42 eV and 10^6 cm^{-3}, respectively. In order to generate electron hole pairs in GaAs, which one of the wavelength (λ_C) ranges of incident radiation, is most suitable? (Given that : Plank's constant is 6.62×10^{-34} J-s, velocity of light is 3×10^{10} cm/s and charge of electron is 1.6×10^{-19}C)

(a) $0.42\ \mu m < \lambda_C < 0.87\ \mu m$ (b) $0.87\ \mu m < \lambda_C < 1.42\ \mu m$

(c) $1.42\ \mu m < \lambda_C < 1.62\ \mu m$ (d) $1.62\ \mu m < \lambda_C < 6.62\ \mu m$

GATE(EC-IV/2014/1M)

Solution : Ans (a)

The wavelength of radiation for generation of electron-hole pair is given by,

$$\lambda < \frac{1.24}{E_g} \mu m$$

$$\Rightarrow \quad \lambda < \frac{1.24}{1.42} \mu m$$

$$\Rightarrow \quad \lambda < 0.87\ \mu m$$

❐❐❐

GATE QUESTIONS

Q.1 The band gap of Silicon at room temperature is

(a) 1.3 eV (b) 0.7 eV

(c) 1.1 eV (d) 1.4 eV

GATE(EC/2005/1M)

Q.2 The primary reason for the widespread use of Silicon in semiconductor device technology is

(a) abundance of Silicon on the surface of the Earth

(b) larger band gap of Silicon in comparison to Germanium

(c) favorable properties of Silicon-dioxide (SiO2)

(d) lower melting point

GATE(EC/2005/1M)

Q.3 A long specimen of p-type semiconductor material

(a) is positively charged (b) is electrically neutral

(c) has an electric field directed along its length (d) acts as a dipole

GATE(EC/1998/1M)

Q.4 n-type silicon is obtained by doping silicon with

(a) Germanium (b) Aluminum

(c) Boron (d) Phosphorus

GATE(EC/2003/1M)

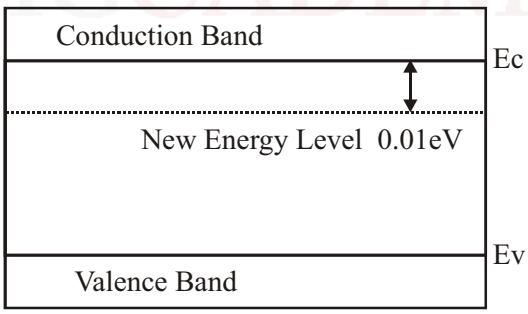
Q.5 In an n-type silicon crystal at room temperature, which of the following can have a concentration of 4×10^{19} cm^{-3} ?

(a) Silicon atoms (b) Holes

(c) Dopant atoms (d) Valence electrons

GATE(EC/2009/1M)

Q.6 A small percentage of impurity is added to an intrinsic semiconductor at 300 K. Which one of the following statements is true for the energy band diagram shown in the following figure?



(a) Intrinsic semiconductor doped with pentavalent atoms to form n-type semiconductor

(b) Intrinsic semiconductor doped with trivalent atoms to form n-type semiconductor

(c) Intrinsic semiconductor doped with pentavalent atoms to form p-type semiconductor

(d) Intrinsic semiconductor doped with trivalent atoms to form p-type semiconductor

GATE (EC-I/2016/1M)

Q.7 A bar of Gallium Arsenide (GaAs) is doped with Silicon such that the Silicon atoms occupy Gallium and Arsenic sites in the GaAs crystal. Which one of the following statement is true?

(a) Silicon atoms act as p-type dopants in Arsenic sites and n-type dopants in Gallium sites

(b) Silicon atoms act as n-type dopants in Arsenic sites and p-type dopants in Gallium sites

(c) Silicon atoms act as p-type dopants in Arsenic as well as Gallium sites

(d) Silicon atoms act as n-type dopants in Arsenic as well as Gallium sites

GATE(EC-I/2017/1M)

Q.8 The intrinsic carrier concentration of silicon sample at 300 K is $1.5\times10^{16}/m^3$. If after doping, the number of majority carriers is $5\times10^{20}/m^3$, the minority carrier density is

(a) $4.50\times10^{11}/m^3$ (b) $3.33\times10^{5}/m^3$

(c) $5.00\times10^{20}/m^3$ (d) $3.00\times10^{-5}/m^3$

GATE(EC/2003/1M)

Q.9 The concentration of minority carriers in an extrinsic semiconductor under equilibrium is

(a) Directly proportional to the doping concentration

(b) Inversely proportional to the doping concentration

(c) Directly proportional to the intrinsic concentration

(d) Inversely proportional to the intrinsic concentration

GATE(EC/2006/1M)

Q.10 A silicon sample is uniformly doped with 10^{16} phosphorous atoms/cm^3 and 2×10^{16} boron atoms/cm^3. If all the dopants are fully ionized, the material is

(a) n-type with carrier concentration of $10^{16}cm^{-3}$

(b) p-type with carrier concentration of $10^{16}cm^{-3}$

(c) n-type with carrier concentration of $2\times10^{16}cm^{-3}$

(d) p-type with carrier concentration of $2\times10^{-16}cm^{-3}$

GATE(EC/1991/2M)

Q.11 In a p -type silicon sample, the hole concentration is $2.25\times10^{15}/cm^3$. If the intrinsic carrier concentration is $1.5\times10^{10}/cm^3$,the electron concentration is

(a) zero (b) $10^{10}/cm^3$

(c) $10^{5}/cm^3$ (d) $1.5\times10^{25}/cm$

GATE(EC/1995/1M)

Q.12 The intrinsic carrier density at 300 K is $1.5\times10^{10}/cm^3$, in silicon. For n-type silicon doped to 2.25×10^{15} atoms/cm^3, the equilibrium electron and hole densities are

(a) $n = 1.5\times10^{15}/cm^3$, $p = 1.5\times10^{10}/cm^3$ (b) $n = 1.5\times10^{10}/cm^3$, $p = 2.25\times10^{15}/cm^3$

(c) $n = 2.25\times10^{15}/cm^3$, $p = 1.0\times10^{5}/cm^3$ (d) $n = 1.5\times10^{10}/cm^3$, $p = 1.5\times10^{10}/cm^3$

GATE(EC/1997/2M)

Q.13 The electron and hole concentrations in a intrinsic semiconductor are n_i and p_i respectively. Then

(a) $n + p = n_i + p_i$ (b) $n + n_i = p + p_i$

(c) $np_i = n_i p$ (d) $np = n_i p_i$

GATE(EC/1998/1M)

Q.14 The electron and hole concentrations in an intrinsic semiconductor are n_i per cm^3 at 300 K. Now, if acceptor impurities are introduced with a concentration of N_A per cm^3 (where $N_A >> n_i$) , the electron concentration per cm^3 at 300 K will be

(a) n_i (b) n_i+N_A

(c) N_A (d) $\frac{n_i^2}{N_A}$

GATE(EC/2007/1M)

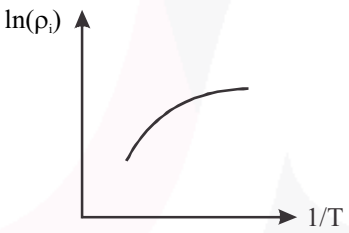
Q.15 A silicon sample A is doped with 10^{18} atoms/cm^3 of Boron. Another sample B of identical dimensions is doped with 10^{18} atoms/cm^3 of Phosphorus. The ratio of electron to hole mobility is 3. The ratio of conductivity of the sample A to B is

(a) 3 (b) 1/3

(c) 2/3 (d) 3/2

GATE(EC/2005/2M)

Q.16 In the figure, In (ρ_i) is plotted as a function of 1/T, where ρ_i si the intrinsic resistivity of silicon, T is the temperature, and the plot is almost linear.



The slope of the line can be used to estimate

(a) band gap energy of silicon (E_g)

(b) sum of electron and hole mobility in silicon ($\mu_n + \mu_p$)

(c) reciprocal of the sum of electron and hole mobility in silicon $(\mu_n + \mu_p)^{-1}$

(d) intrinsic carrier concentration of silicon (n_i)

GATE(EC-IV/2014/1M)

Q.17 Under high electric fields, in a semiconductor with increasing electric field

(a) The mobility of charge carriers decreases (b) The mobility of charge carriers increases

(c) The velocity of the charge carriers saturates (d) The velocity of the charge carriers increases.

GATE(EC/1990/2M)

Q.18 An n-type silicon sample, having electron mobility μ_n equal to twice the hole mobility μ_p, is subjected to a steady illumination such that the electron concentration doubles from its thermal equilibrium value. As a result, the conductivity of the sample increases by a factor of...

(a) 2 (b) 4

(c) 6 (d) 2.5

GATE(EC/1991/2M)

Q.19 A small concentration of minority carriers is injected into a homogeneous semiconductor crystal at one

point. An electric field of 10 V/cm is applied across the crystal and this moves the minority carriers a distance of 1 cm in 20 μ sec. The mobility (in $cm^2/V\text{-}s$) will be

(a) 1, 000 (b) 2, 000

(c) 5, 000 (d) 500,000

GATE(EC/1994/1M)

Q.20 The drift velocity of electrons, in silicon

(a) Is proportional to the electric field for all values of electric field

(b) Is independent of the electric field

(c) Increases at low values of electric field and decreases at high values of electic field exhibiting negative differential resistance

(d) Increases linearly with electric field at low values of electric field and gradually saturates at higher values of electric field.

GATE(EC/1995/1M)

Q.21 A silicon sample is uniformly doped with donor type impurities with a concentration of $10^{16}/cm^3$. The electron and hole mobilities in the sample are 1200 $cm^2/V\text{-}s$ and 400 $cm^2/V\text{-}s$ respectively.

Assume complete ionization of impurities. The charge of an electron is 1.6×10^{-19} C. The resistivity of the sample (in Ω-cm) is .....

GATE(EC-I/2015/1M)

Q.22 A thin P-type silicon sample is uniformly illuminated with light which generates excess carriers. The recombination rate is directly proportional to

(a) the minority carrier mobility (b) the minority carrier recombination lifetime

(c) the majority carrier concentration (d) the excess minority carrier concentration

GATE(EC-III/2014/1M)

Q.23 A semiconductor is irradiated with light such that carriers are uniformly generated throughout its volume. The semiconductor is n-type with $N_D = 10^{19}$ per cm^3. If the excess electron concentration in the steady state is $\Delta n = 10^{15}$ per cm^3 and if $\tau_p = 10\mu$ sec [minority carrier life time] the generation rate due to irradiation

(a) is 102^0 e-h pairs/cm^3/s (b) is 101^0 e-h pairs/cm^3/s

(c) is 102^4 e-h pairs/cm^3/s (d) cannot be determined as the data is insufficient.

GATE(EC/1992/2M)

Q.24 The units of $\frac{q}{kT}$ are

(a) V (b) V^{-1}

(c) J (d) J/K

GATE(EC/1998/1M)

Q.25 The ratio of the mobility to the diffusion coefficient in a semiconductor has the units

(a) V^{-1} (b) $cm \cdot V^{-1}$

(c) $V \cdot cm^{-1}$ (d) $V \cdot s$

GATE(EC/2009/1M)

Q.26 The electron concentration in a sample of uniformly doped n-type silicon at 300 K is $2.25\times10^{15}/cm^3$. If the charge of an electron is 1.6×10^{-19} coulomb and the diffusion constant $D_n = 35$ cm^2/s, the current

density in the silicon, if no electric field is present, is

(a) zero
(b) $-1120\ A/cm^2$
(c) $+1120\ A/cm^2$
(d) $-1120\ A/cm^2$

GATE(EC/2003/2M)

Q.27 Under low level injection assumption, the injected minority carrier current for an extrinsic semiconductor is essentially the

(a) Diffusion current
(b) Drift current
(c) Recombination current
(d) Induced Current

GATE(EC/2006/1M)

Q.28 Drift current in semiconductors depends upon

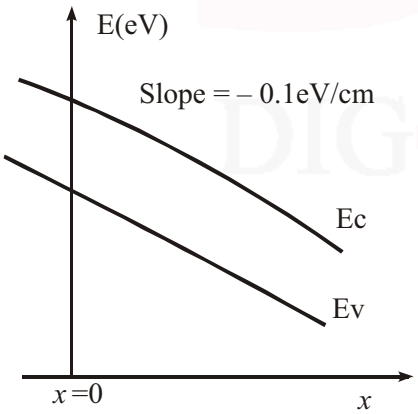
(a) only the electric field
(b) only the carrier concentration gradient
(c) both the electric field and the carrier concentration
(d) both the electric field and the carrier concentration gradient

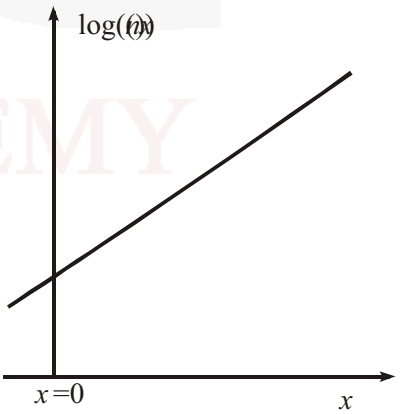
GATE(EC/2011/1M)

Q.29 Assume electronic charge $q = 1.6 \times 10^{-19}$ C,kT/q = 25m V and electron mobility $\mu_n = 1000\ cm^2/V\text{-}s$. If the concentration gradient of electrons injected into a P-type silicon sample is $1 \times 10^{21}/cm^3$, the magnitude of electron diffusion current density (in A/cm^2) is_____

GATE(EC-II/2014/2M)

Q.30 The energy band diagram and the electron density profile $n(x)$ in a semiconductor are shown in the figures. Assume that $n(x) = 10^{15}\ e^{\left(\frac{q\alpha x}{kT}\right)}\ cm^{-3}$, with $\alpha = 0.1$ V/cm and x expressed in cm. Given $\frac{kT}{q}$ = 0.026 V, $D_n = 36\ cm^2\ s^{-1}$, and $\frac{D}{\mu} = \frac{kT}{q}$. The electron current density (in A/cm^2) at $x = 0$ is



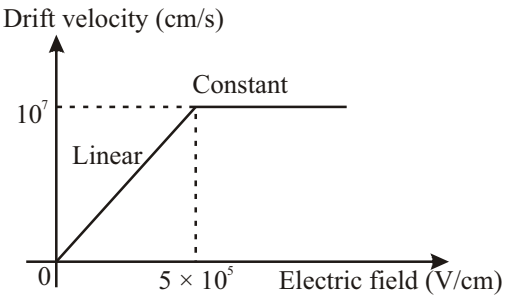


(a) $-4.4 \times 10 -2$
(b) $-2.2 \times 10-2$
(c) 0
(d) $2.2 \times 10-2$

GATE(EC-II/2015/2M)

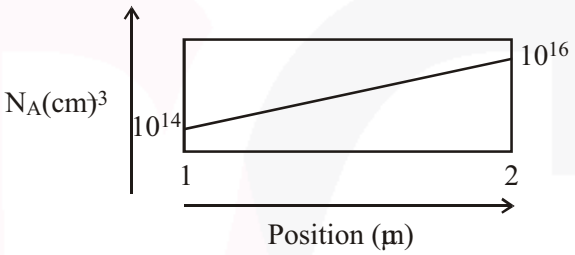
Q.31 The dependence of drift velocity of electrons on electric field in a semiconductor is shown below.

The semiconductor has a uniform electron concentration of $n = 1 \times 10^{16}$ cm^{-3} and electronic charge $q = 1.6 \times 10^{-19}$ C. If a bias of 5V is applied across a 1 μm region of this semiconductor, the resulting current density in this region, in kA/cm^2, is _____.



GATE(EC-I/2017/2M)

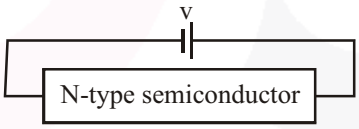
Q.32 The figure below shows the doping distribution in a *p*-type semiconductor in log scale.



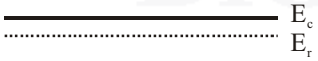
The magnitude of the electric field (in kV/cm) in the semiconductor due to non uniform doping is .....

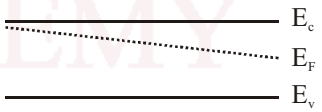
GATE(EC-I/2016/2M)

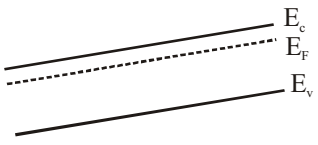
Q.33 An N-type semiconductor having uniform doping is biased as shown in the figure.

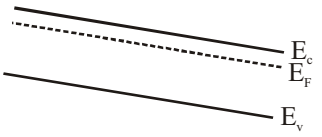


if E_C is the lowest energy level of the conduction band, E_V is the highest energy level of the valance band and E_F is the Fermi level, which one of the following represents the energy band diagram for

(a)


(b)


(c)


(d)


GATE (EC-IV/2014/2M)

Q.34 The probability that an electron in a metal occupies the Fermi-level at any temperature (> 0°K)

(a) 0 (b) 1

(c) 0.5 (d) 1.0

GATE(EC/1995/1M)

Q.35 The majority carriers in an n - type semiconductor have an average drift velocity v in a direction perpendicular to a uniform magnetic field B. The electric field E induced due to Hall effect acts in the direction

(a) $v \times B$ (b) $B \times v$

(c) along v (d) opposite to v

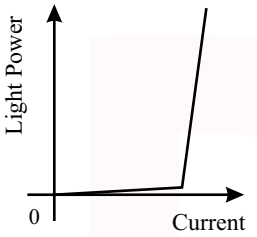
GATE(EC/2006/2M)

Q.36 The cut-off wavelength (in μm) of light that can be used for intrinsic excitation of a semiconductor material of band gap $E_g = 1.1$ eV is_____

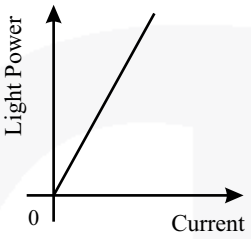
GATE(EC-IV/2014/1M)

Q.37 Correct input - output characteristic curve of a semiconductor laser is

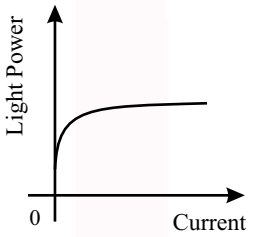
(a)



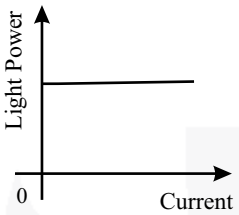
(b)



(c)



(d)



GATE(IN/2006/1M)

Q.38 A single crystal intrinsic semiconductor is at a temperature of 300 K with effective density of states for holes twice that of electrons. The thermal voltage is 26 mV. The intrinsic Fermi level is shifted from mid-bandgap energy level by

(a) 18.02 meV (b) 9.01 meV

(c) 13.45 meV (d) 26.90 meV

GATE(EC/2020/1M)

Q.39 A bar of silicon is doped with boron concentration of 10^{16} cm^{-3} and assumed to be fully ionized. It is exposed to light such that electron-hole pairs are generated throughout the volume of the bar at the rate of 10^{20} cm^{-3} s^{-1}. If the recombination lifetime is 100 μs, intrinsic carrier concentration of silicon is 10^{10} cm^{-3} and assuming 100% ionization of boron, then the approximate product of steady-state electron and hole concentrations due to this light exposure is

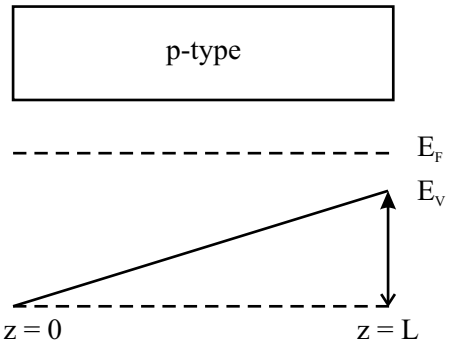
(a) 10^{20} cm^{-6} (b) 2×10^{20} cm^{-6}

(c) 10^{32} cm^{-6} (d) 2×10^{32} cm^{-6}

GATE(EC/2021/1M)

Q.40 The energy band diagram of a p-type semiconductor bar of length L under equilibrium condition (i.e., the Fermi energy level E_F is constant) is shown in the figure. The valance band E_X is sloped since doping is non-uniform along the bar. The difference between the energy levels of the valence band at

the two edges of the bar is Δ.



If the charge of an electron is q, then the magnitude of the electric field developed inside this semiconductor bar is

(a) $\frac{\Delta}{qL}$

(b) $\frac{2\Delta}{qL}$

(c) $\frac{\Delta}{2qL}$

(d) $\frac{3\Delta}{2qL}$

GATE(EC/2021/1M)

❐❐❐

Answers & Explanations OF GATE Questions

Q.1 ***Ans.(c)***

The energy band gap in the Si is function of temperature as temperature increases the band gap energy decreases.

$$E_g(T) = 1.21 - 3.60 \times 10^{-4}T \text{ eV}$$

At $T = 300$ K

$$E_g(300\text{ K}) = 1.21 - 3.60 \times 10^{-4} \times 300 \text{ eV} = 1.102 \text{ eV}$$

Note:- For Ge, $E_g(T) = 0.785 - 2.23 \times 10^{-4}T$ eV

Q.2 ***Ans.(c)***

Advantages of Silicon for use in semiconductor Technology,

1. Higher melting point 1240 °C as compared to 937 °C of Ge.
2. Abundant & inexpensive source
3. Larger band gap
4. Excellent insulating property of SiO_2
5. Better heat conductivity.
6. Nontoxic

But favorable properties of SiO_2 is the main reason for using Si in semiconductor device technology.

Q.3 ***Ans.(b)***

All semiconductors intrinsic as well as extrinsic are always electrically neutral.

$$\therefore \quad n + N_d = p + N_a$$

Q.4 ***Ans.(d)***

Donor or n-type impurities : P, As, Sb & Bi

Note: Acceptor impurities :B, Al, Ga & In

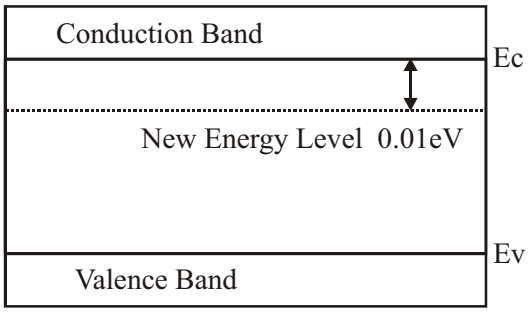
Q.5 ***Ans.(c)***

Concentration of atoms in Si = 5×10^{22} cm^{-3}

Intrinsic carrier concentration, $n_i = 2.5 \times 10^{13} cm^{-3}$

In n-type semiconductors the concentration of minority carriers is less than the concentration of majority carriers. So given concentration can not be concentration of holes. Therefore, the concentration of 4×10^{19} cm^{-3} can be that of dopant atoms.

Q.6 **Ans. (*a*)**



When an intrinsic semiconductor doped with penta-valent atoms to form n-type semiconductor the energy level of impurity is close to the conduction band. Thus given energy band diagram is for n-type semiconductor.

Q.7 Ans.(a)

A bar of Gallium Arsenide (GaAs) is doped with Silicon can behave both n-type or p-type of semiconductors depending on which site is occupied by Si. It haves as donor impurity when it replaces Ga atom and it behaves as acceptor impurity when it replaces the As atom. So, material is n-type when Si atom replaces the Ga and it p-type when Si atom replaces As atom.

Q.8 Ans.(a)

Let the doping impurity is n-type.

The concentration of majority carriers,

$$n_n \approx N_D = 5\times10^{20}/cm^3$$

The concentration of minority carriers,

$$p_n = \frac{n_i^2}{N_D}$$

$$\Rightarrow \quad p_n = \frac{\left(1.5\times10^{16}\right)^2}{\left(5\times10^{20}\right)} = 4.5\times10^{11}\ /m^3$$

Q.9 Ans.(b)

The concentration of holes in n-type semiconductors,

$$p_n = \frac{n_i^2}{N_D} \qquad .....(i)$$

And the concentration of electrons in p-type semiconductors,

$$n_p = \frac{n_i^2}{N_A} \qquad .....(ii)$$

From the equation (i) & (ii) it is clear that the concentration of minority carriers in an extrinsic semiconductor under equilibrium is inversely proportional to the doping concentration.

Q.10 Ans.(b)

When material is doped with both types of impurity resultant material may be either p-type or n-type depending on level of doping with acceptor and donor impurities.

Case-I: $N_D > N_A$

Then resultant material is n-type with,

$$n_n \approx N_D - N_A$$

and $$p_n = \frac{n_i^2}{N_D - N_A}$$

Case-II: $N_A > N_D$

Then resultant material is p-type with,

$$p_p \approx N_A - N_D$$

And $$n_p = \frac{n_i^2}{N_A - N_D}$$

Given, $N_D = 10^{16}\text{cm}^{-3}$,

$N_A = 2 \times 10^{16}\text{cm}^{-3}$

Since $N_A > N_D$, therefore given sample is p-type with carrier concentration of $(2 \times 10^{16} - 10^{16})$ or 10^{16}cm^{-3}.

Q.11 Ans.(c)

The concentration of holes in p-type semiconductors,

$$p_p \approx N_A = 2.25\times10^{15}\ /\text{cm}^3$$

The concentration of electrons in p-type semiconductors,

$$n_p = \frac{n_i^2}{N_A}$$

$$\Rightarrow \quad n_p = \frac{\left(1.5\times10^{10}\right)^2}{\left(2.25\times10^{15}\right)} = 10^5\ /\text{cm}^3$$

Q.12 Ans.(c)

The concentration of electrons in n-type semiconductors,

$$n_n \approx N_D = 2.25\times10^{15}\ /\text{cm}^3$$

The concentration of holes in n-type semiconductors,

$$p_n = \frac{n_i^2}{N_D}$$

$$\Rightarrow \quad p_n = \frac{\left(1.5\times10^{10}\right)^2}{\left(2.25\times10^{15}\right)} = 10^5\ /\text{cm}^3$$

Q.13 Ans.(d)

For intrinsic semiconductors, $n_i = p_i$

According to law of mass action,

$$np = n_i^2$$

Q.14 Ans.(d)

According to law of mass action,

$$np = n_i^2$$

For p-type semiconductor having acceptor impurities, $p \approx N_A$

$$\Rightarrow \quad n = \frac{n_i^2}{p} = \frac{n_i^2}{N_A}$$

Q.15 Ans.(b)

Given, $N_A = 10^{18}$ atoms/cm^3 ;

$N_D = 10^{18}$ atoms/cm^3 ;

$\frac{\mu_n}{\mu_p} = 3$

Conductivity of extrinsic semiconductors,

$$\sigma = e(p\mu_p + n\mu_n)$$

For p-type semiconductors, $p >> n$ & $p \approx N_A$

$$\therefore \quad \sigma_A \approx N_A e\mu_p \qquad .....(i)$$

For n-type semiconductors, $n >> p$ & $n \approx N_D$

$$\therefore \quad \sigma_B \approx N_D e\mu_n \qquad .....(ii)$$

From equation (i) & (ii),

$$\frac{\sigma_A}{\sigma_B} = \frac{N_A q\mu_p}{N_D q\mu_n} = \frac{1}{3}$$

Q.16 Ans (a)

The conductivity of intrinsic semiconductor is given by,

$$\sigma = en_i(\mu_n + \mu_p)$$

The intrinsic concentration of charge carriers of the semiconductor is given by

$$n_i = A_o T^{3/2} e^{-\frac{E_{g0}}{2kT}}$$

Where A_o is a constant, T is temperature in K and E_{go} is bank gap at 0 K

$$\therefore \quad \sigma = e A_o T^{3/2} e^{-\frac{E_{g0}}{2kT}} \left(\mu_n + \mu_p\right)$$

Intrinsic resistivity of semiconductor is related to conductivity as

$$\rho_i = \frac{1}{\sigma_i}$$

$$\Rightarrow \quad \rho_i = \frac{1}{e A_o T^{3/2} e^{-\frac{E_{g0}}{2kT}} (\mu_n + \mu_p)}$$

$$\Rightarrow \quad \rho_i = \frac{1}{e A_0 T^{3/2} (\mu_n + \mu_p)} e^{\frac{E_{g0}}{2kT}}$$

Taking log on both sides,

$$\Rightarrow \ln \rho_i = \ln\left(e^{+\frac{E_{g0}}{2kT}} \right) - \ln\left(e A_0 T^{3/2} (\mu_n + \mu_p) \right)$$

$$\Rightarrow \ln \rho_i = \frac{E_{g0}}{2k} \frac{1}{T} - \ln\left(e A_0 T^{3/2} (\mu_n + \mu_p) \right)$$

$$\Rightarrow \quad y = mx + c \qquad \text{.....(i)}$$

Where, $y = \ln \rho_i$, $m = \frac{E_{go}}{2k}$, $x = \frac{1}{T}$ and

$$c = -\ln\left(e A_0 T^{3/2} (\mu_n + \mu_p) \right)$$

Equation (i) represents equation of straight line of $\ln \rho_i$ Vs $\frac{1}{T}$ with slope of the line equal to $\frac{E_{go}}{2k}$

So, the slope of line can be used to determine the band gap energy of intrinsic semiconductor.

Q.17 **Ans.(a, c)**

Drift velocity,

$$v_d = \mu E$$

And

μ = constant for $E < 10^3$ V/cm

$\mu \propto E^{-1/2}$ for $10^3 < E < 10^4$ V/cm

$\mu \propto E^{-1}$ for $E > 10^4$ V/cm

Therefore,

$v_d \propto E$ for $E < 10^3$ V/cm

$v_d \propto E^{+1/2}$ for $10^3 < E < 10^4$ V/cm

v_d = constant for $E > 10^4$ V/cm

Thus at higher fields the mobility decreases and drift velocity saturates with increase in field.

Q.18 ***Ans.(d)***

Conductivity of extrinsic semiconductors,

$$\sigma = e(p\mu_p + n\mu_n)$$

for n-type semiconductors, n >> p

$$\therefore \quad \sigma \approx ne\mu_n$$

The illumination of the semiconductor results in generation of electron hole pairs. If concentration of electrons is doubled increases from n to 2n then concentration of holes changes from p to p + n.

then, $\sigma_1 = e[(p+n)\mu_p + 2n\mu_n]$

$$\approx e(n\mu_p + 2n\mu_n)$$

Given $\mu_n = 2\mu_p$ or $\mu_p = 0.5\mu_n$

$\Rightarrow$ $\sigma_1 = e(0.5n\mu_n + 2n\mu_n)$

$$= 2.5\, ne\mu_n = 2.5\sigma$$

Q.19 Ans.(c)

Drift velocity, $v_d = \dfrac{\text{distance travelled}}{\text{time taken}}$

$$= \frac{1\,cm}{20\,\mu\text{sec.}}$$

$$v_d = 0.05 \times 10^6\,\text{cm/sec}$$

Mobility, $\mu = \dfrac{v_d}{E} = \dfrac{0.05}{10} \times 10^6 = 5000\ \text{cm}^2\text{/V-s}$

Q.20 Ans.(d)

Drift velocity, $v_d = \mu E$

And μ = constant for $E < 10^3$ V/cm

$\mu \propto E^{-1/2}$ for $10^3 < E < 10^4$ V/cm

$\mu \propto E-1$ for $E > 10^4$ V/cm

Therefore,

$v_d \propto E$ for $E < 10^3$ V/cm

$v_d \propto E+ 1/2$ for $10^3 < E < 10^4$ V/cm

v_d = constant for $E > 10^4$ V/cm

***Q.21* Ans. 0.50 to 0.54**

Conductivity of extrinsic semiconductors,

$$\sigma = e(p\mu_p + n\mu_n)$$

For n-type semiconductors, n >> p

$\therefore \quad \sigma \approx ne\mu_n$

$\Rightarrow \quad \sigma = 10^{16} \times 1.6 \times 10^{-19} \times 1200$

$\Rightarrow \quad \sigma = 10^{16} \times 1.6 \times 10^{-19} \times 1200$

Resistivity, $\rho = \frac{1}{\sigma} = \frac{1}{10^{16} \times 1.6 \times 10^{-19} \times 1200}$

$\Rightarrow \quad \rho = 0.52\ \Omega\text{-cm})$

Q.22 Ans (d)

When a P-type silicon sample is uniformly illuminated with light which generates excess carriers the recombination rate is directly proportional to the excess minority carrier concentration.

Q.23 Ans.(d)

The excess majority carrier generation under uniform illumination of n-type sample is given by,

$$n' = g_{op}\tau_n$$

Where g_{op} is called optical generation rate and τ_n is average life time of majority carriers.

$\Rightarrow \quad g_{op} = \frac{n'}{\tau_n}$

Here, τ_n is average life time of majority carriers (τ_n) is not given so the data is insufficient.

Q.24 Ans.(b)

As per Einstein relationship,

$$\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = V_T = \frac{KT}{q} = \frac{T}{1600}$$

Where, V_T is called *thermal voltage,* μ_n & μ_p are mobilities and D_n & D_p are the diffusion constants.

$\Rightarrow \quad \frac{q}{kT} = \frac{1}{V_T}$

Thus units of $\frac{q}{kT}$ are V^{-1}

Q.25 Ans.(a)

As per Einstein relationship,

$$\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = V_T = \frac{KT}{q} = \frac{T}{1600}$$

Where, V_T is called *thermal voltage,* μ_n & μ_p are mobilities and D_n & D_p are the diffusion constants.

$\Rightarrow \quad \frac{\mu_p}{D_p} = \frac{1}{V_T}$

The ratio of the mobility to the diffusion coefficient in a semiconductor has the units of V^{-1}.

Q.26 Ans.(a)

Note that the sample is uniformly doped so there is no concentration gradient.

$$\therefore \quad \frac{\partial n}{\partial x} = 0$$

Then diffusion current density,

$$J_{n,diff} = q D_n \frac{\partial n}{\partial x} = 0$$

Since electric field is zero ,therefore, drift current density,

$$J_{n,drift} = 0$$

Total current density,

$$J_n = J_{n,diff} + J_{n,drift} = 0$$

Q.27 Ans.(a)

Under low level injection assumption, the injected minority carrier current for an extrinsic semiconductor is essentially the diffusion current.

Q.28 Ans.(c)

The drift current density in a semiconductors is given by,

$$J_{drift} = \sigma E$$

Where,

$\sigma = q(n\mu_n + p\mu_p)$ = conductivity

n = Concentration of electrons

p = Concentration of holes

μ_n , $\mu_p \rightarrow$ Mobilities of electrons and holes.

So, drift current depends on,

i) Electric field

ii) Concentration of charge carriers

iii) Mobility of charge carriers.

Q.29 Ans.(3990 to 4010)

Given, $\frac{kT}{q} = 25mV$, $\mu_n = 1000\ c.m^2/V.s$

According to Einstein relation,

$$\frac{D_n}{\mu_n} = \frac{kT}{q}$$

$$\Rightarrow \quad D_n = \frac{kT}{q}\mu_n$$

$\Rightarrow \quad D_n = 25 \times 10^{-3} \times 1000 = 25\ cm^2/s$

The diffusion current density due to electrons in p-type sample is given by,

$$J_n = q D_n \frac{dn}{dx}$$

Given, $\frac{dn}{dx} = 1 \times 10^{21}\ cm^{-3}.$

$\Rightarrow \quad J_n = 1.6 \times 10^{-19} \times 25 \times 10^{21}\ A/cm^2$

$\Rightarrow \quad J_n = 4000\ A/cm^2$

Q.30 **Ans.(*c*)**

Given, $n(x) = 10^{15}\, e^{\left(\frac{q\alpha x}{kT}\right)}\ cm^{-3}$

$$\frac{dn(x)}{dx} = 10^{15} \frac{q\alpha}{kT} e^{\frac{q\alpha x}{kT}}$$

The electron current density due to concentration gradient is given by,

$$J_n = q D_n \frac{dn(x)}{dx}$$

$\Rightarrow \quad J_n = q D_n \times 10^{15} \frac{q\alpha}{kT} . e^{\frac{q\alpha x}{kT}}$

At x = 0, $J_n = q D_n \times 10^{15} \frac{q\alpha}{kT}$

Given, $\frac{kT}{q} = 0.026$

$D_n = 36\ cm^2/s,$

$\alpha = 0.1\ V/cm$

$\Rightarrow \quad J_n = 1.9 \times 10^{-19} \times 36 \times 10^{15} \times \frac{0.1}{0.026}$

$\Rightarrow \quad J_n = 2.2 \times 10^{-2}\ A/cm^2$

Note : Answer given in GATE Answer key is (c)

Q.31 ***Ans. : 1.5 to 1.7***

Given length of region of semiconductor,

$L = 1\ \mu m$

Bias voltage, $V = 5V,$

Concentration of electrons,

$$n = 1 \times 10^{16}\ cm^{-3}$$

Electric field across the region,

$$E = \frac{V}{L} = \frac{5}{1\times10^{-6}} = 5\times10^{6}\ V/m$$

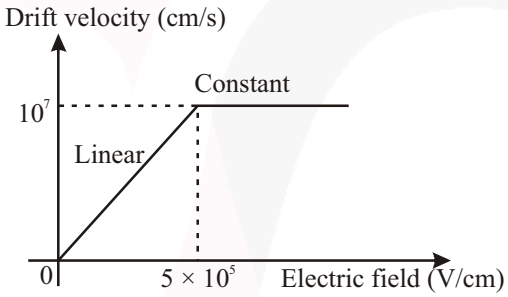
or $$E = 5 \times 10^{4}\ V/c.m.$$

The draft velocity of electrons,

$$v_d = \mu_n E$$

$$\Rightarrow \quad \mu_n = \frac{v_d}{E} \qquad .....(i)$$

If a curve is drawn between v_d and E then μ_n is slope of the curve.



The slope of v_d Vs E given curve,

$$\mu_n = \frac{10^7}{5\times10^5}$$

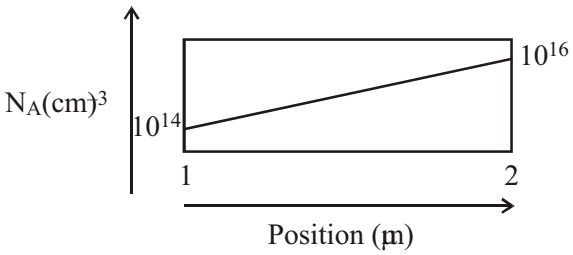
$$\Rightarrow \quad \mu_n = 20\ cm^2/V\text{-}s$$

$\therefore$ Drift current density in the region of bias voltage,

$$J = \sigma E = ne\mu_n E$$

$$\Rightarrow \quad J = 1\times10^{16}\times1.6\times10^{-19}\times20\times5\times10^{4} = 1.6\ kA/cm^2$$

Q.32 **Ans. 1.10:1.25**



The concentration gradient in the bar shown above results in diffusion current. The total current inside open circuited bar is always zero. So, to counter balance the diffusion current a voltage is induced between ends of the bar which causes an equal and opposite drift current. So net current

inside the bar is zero.

$$I_{p,\,\text{diff}} + I_{p,\,\text{drift}} = 0$$

$$\Rightarrow \quad -e D_p \frac{dp}{dx} + e\mu_p p E = 0$$

$$\Rightarrow \quad E = \frac{1}{p}\left(\frac{D_p}{\mu_p}\right)\frac{dp}{dx}$$

As per Einstein relation,

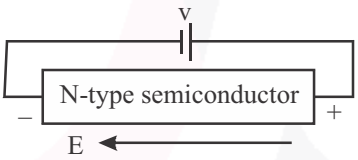
$$\frac{D_p}{\mu_p} = V_T$$

$$\Rightarrow \quad E = \frac{V_T}{p}.\frac{dp}{dx}$$

For p-type material, $p \approx N_A$

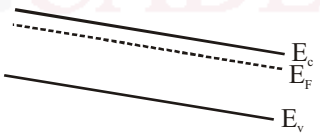
$$\Rightarrow \quad E = \frac{V_T}{N_A}.\frac{dN_A}{dx}$$

Q.33 ***Ans (d)***



The charge carriers always move form region of higher potential energy to the region of lower potential energy. The potential energy decreases in direction of electric field or it increases in the opposite direction of electric field.

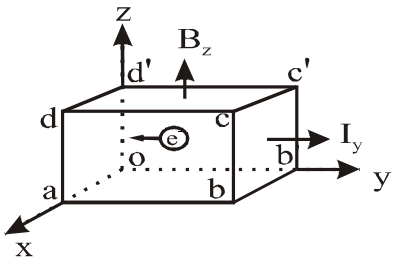
Inside the given semiconductor bar the electric field is directed from positive terminal to negative terminals and thus potential energy decreases from region of negative potential to positive potential inside the bar as shown below,



Q.34 ***Ans.(c)***

The probability of occupying Fermi level at any temperature in metals 50%.

Q.35 **Ans.(b)**



Force experienced by electrons,

$$\vec{F} = q\left(\vec{v}\times\vec{B}\right)$$

Here, $q = -e$

$$\vec{v} = -v_y\hat{a}_y$$

$$\vec{B} = B_z\hat{a}_z$$

$$\Rightarrow \quad \vec{F} = -e[(-v_y\hat{a}_y)\times(B_z\hat{a}_z)]$$

$$\Rightarrow \quad \vec{F} = ev_yB_z\left(\hat{a}_y\times\hat{a}_z\right) = ev_yB_z\,\hat{a}_x$$

The electrons experience force in +x-direction and the face abcd becomes negative. So the direction of electric field is + x-direction.

$$\vec{v}\times\vec{B} = (-v_y\hat{a}_y)\times(B_z\hat{a}_z) = -v_yB_z\left(\hat{a}_y\times\hat{a}_z\right) = -v_yB_z\,\hat{a}_x$$

The direction of $\vec{v}\times\vec{B}$ is –x-direction and $\vec{B}\times\vec{v}$ is + x-direction witch is the same direction as that of electric field induced.

So the electric field is induced in direction of $\vec{v}\times\vec{B}$.

Q.36 **Ans : 1.12 to 1.14**

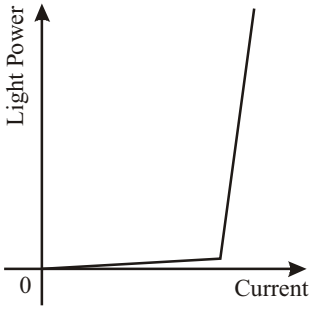
The cut-off wavelength (in μm) of light that can be used for intrinsic excitation of a semiconductor is given by,

$$\lambda_c = \frac{1.24}{E_g}\mu m$$

$$\Rightarrow \quad \lambda_c = \frac{1.24}{1.1}\ \mu m = 1.127\ \mu m$$

Q.37 ***Ans.(a)***

Correct input-output characteristic curve of a semiconductor laser is,



Q.38 Ans(b)

The intrinsic Fermi level in semiconductor with different density of states of electrons & holes is given by,

$$E'_F = \frac{F_C + E_V}{2} + \frac{kT}{2}\ell n\frac{N_V}{N_C}$$

$$\Rightarrow \quad E_F = E_{Fm} + \frac{kT}{2}\ell n\frac{N_V}{N_C}$$

Where $E_{Fm} = \frac{E_C + E_V}{2} =$ midband Fermi level

Shift in Fermi level from midband,

$$E_F - E_{Fm} = \frac{kT}{2}\ell n\frac{N_V}{N_C}$$

Given, $N_V = 2\,N_C$

and $\frac{kT}{q} = 26\text{ kV} = 0.026\text{ V}$

$\therefore \quad kT = 0.026\text{ eV}$

$$\Rightarrow \quad E_F - E_{Fm} = \frac{0.026}{2}\ell n\frac{2N_C}{N_C} = 0.013\,\ell n2$$

$$\Rightarrow \quad E_F - E_{Fm} = 9.01\text{ m eV}$$

Q.39 Ans.(d)

Semiconductor bar doped with boron is a p-type semiconductor.

Given, concentration of baron acceptor impurity,

$$N_A = 10^{16}\text{ cm}^{-3}$$

Concentration of holes when no illumination is applied,

$$p_o \approx N_A = 10^{16}\text{ cm}^{-3}$$

Rate of generation, $g = 10^{20}\text{ cm}^3\text{ s}^{-1}$

Recombination life time, $\tau = 100\ \mu s$

Excess carriers, $\delta p = g\tau = 10^{20} \times 100 \times 10^{-6}\ cm^{-3} = 10^{16}\ cm^{-3}$

Total concentration after illumination,

$$p = p_o + \delta p = 10^{16} + 10^{16} = 2 \times 10^{16}\ cm^{-3}$$

Concentration of electrons before illumination

$$n_o = \frac{n_i^2}{p_o} = \frac{(10^{10})^2}{10^{16}} = 10^4\ cm^{-3}$$

Excess electrons due to illumination,

$$\delta n = \delta p = 10^{16}\ cm^{-3}$$

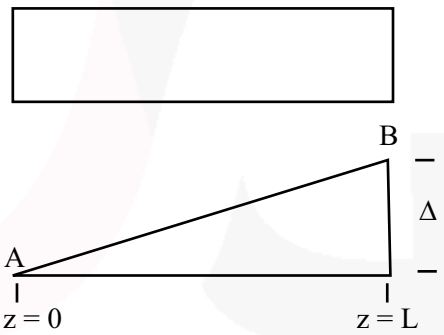
Total concentration of electrons after illumination,

$$n = n_o + \delta n = 10^4 + 10^{16}\ cm^{-3} \approx 10^{16}\ cm^{-3}$$

Product of concentration of electrons and holes after illumination,

$$np = 10^{16} \times 2 \times 10^{16}\ cm^{-6} = 2 \times 10^{32}\ cm^{-6}$$

Q.40 Ans.(a)



Potential difference between ends z = 0 and z = L can be given by

$$V_{AB} = \int_A^B E \cdot d\ell = E.L \qquad .....(i)$$

Where E is electric field

The potential difference developed across the ends of the semiconductor bar due to non-uniform doping can be related to energy difference between two ends of the bar as under,

$$V_{AB} = \frac{W_A - W_B}{q}$$

Where W_A is energy at z = 0 and W_B is energy at z = L.

Given, $W_A - W_B = \Delta$

$\therefore$ $$V_{AB} = \frac{\Delta}{q} \qquad .....(ii)$$

From (i) and (ii), we have,

$$EL = \frac{\Delta}{q}$$

$$\boxed{E = \frac{\Delta}{qL}}$$

❐❐❐

Ch 2 Diodes

2.1. PN Junction

When one side of a semiconductor bar is doped with donor impurity and another side is doped with acceptor impurity there is formation of a p-n junction. During initial process of doping a concentration gradient is formed across the p-n junction. Because the concentration gradient across the junction the holes form p-side of the junction diffuse to n-side and electrons from n-side diffuse to the p-side. During the process the diffusion there is recombination of electron-hole pairs near the junction and bound charges of impurities are uncovered near the junction area. The p-side of the junction is uncovered with negative ions of acceptor impurity and n-side of the junction is uncovered with positive ions of donor impurity as shown in the Fig. 1.

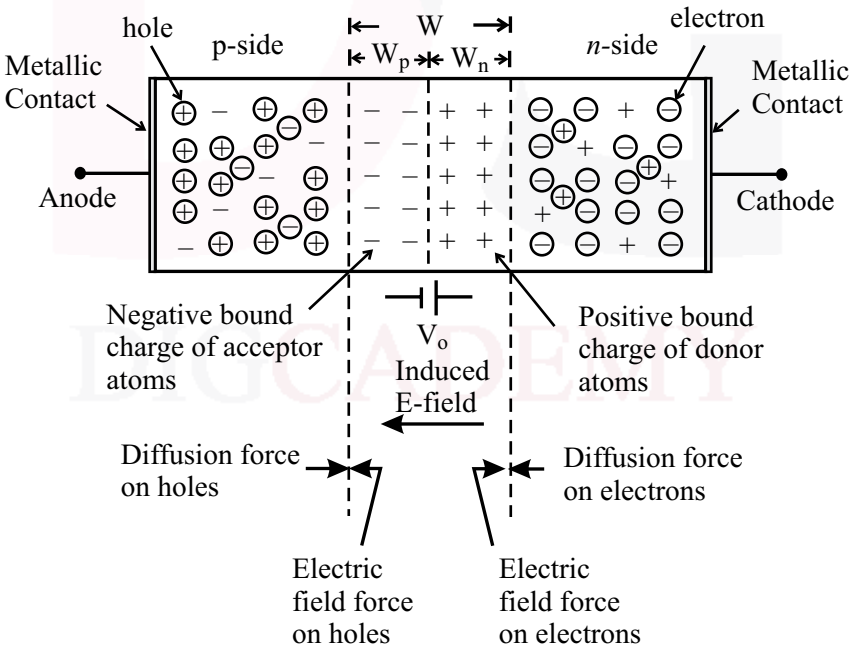


Fig. 1 PN Junction and Space Charge Region

The region in neighborhood of the junction is depleted of free charge carriers. This region is called *depletion region or space charge region or the transition region*. The width of depletion layer is of order of 0.5 μ m for general purpose diode. The depletion region has uncovered positive bound

charges of donor impurity on *n*-side and uncovered negative bound charges of acceptor impurity on p-side. A potential gradient is established in the junction region due to these uncovered bound charges of impurities. At equilibrium the induced potential gradient near junction opposes the diffusion of holes from p-side to n-side and diffusion of electrons from n-side to p-side of the junction. The potential barrier across a step graded pn junction is given by,

$$V_o = V_T \ell n \frac{N_A N_D}{n_i^2} = \frac{kT}{q} \ell n \frac{N_A N_D}{n_i^2} \quad (1)$$

Where, N_A is acceptor concentration on p-side and N_D is donor concentration of n-side of the junction.

Note : *i. When the terminals of a diode are short circuited their is no current across the short circuited terminals because the potential barrier is formed by immobile charges (bound charges) due to which current cannot flow. During short circuited condition their is no current in the diode. But the potential of potential barrier appears across the metallic contacts of the diode.*

ii. Potential barrier of a diode cannot be measured using a voltmeter because voltmeter also require some current to give the deflection but positive bound charges of depletion region are not able to move.

iii. External connection of pn junction diode are made through ohmic metallic contacts.

2.2 Open Circuited pn Junction

When p-n junction is open circuited the net current through the junction is zero. However, there is concentration gradient across the junction which induces diffusion force on the charge carriers. Under equilibrium condition the induced electric field of space charge around the junction induces a force which is equal and opposite to the diffusion force. Hence, no more diffusion takes place across the junction at equilibrium. Therefore, a potential barrier is induced across the junction which opposes the movement of charge carriers across the junction.

2.2.1 Built-in Potential Barrier of Open Circuited pn Junction

When pn junction is open circuited the junction is in thermal equilibrium and the Fermi energy level (E_F) is at same level on both sides of the pn junction. Under thermal equilibrium and open circuited condition of pn junction there is no flow of charge carriers across the junction. For jumping of electron from conduction of n-side to conduction band of p-side, it must climb over a potential hill of value equal to potential barrier of the junction. So, conduction bands on p-side shifts upward and conduction band on n-side shifts downward with total difference of energy of lowest levels on both sides of the junction equal to a value proportional to potential barrier (qV_o) of the junction as shown in the Fig. 2. Similarly, valence band of p-side shifts upward and on n-side shifts downward with a difference proportional to potential barrier (qV_o) of the junction. The intrinsic Fermi level (E_{Fi}) also gets shifted on both sides of the junction by a value equal to potential barrier.

It should be noted here that the conduction band and valence band energy levels are higher on p-side as compared to n-side due to the potential barrier of the junction. The energy level diagram of an open circuited pn junction is shown in Fig. 2.

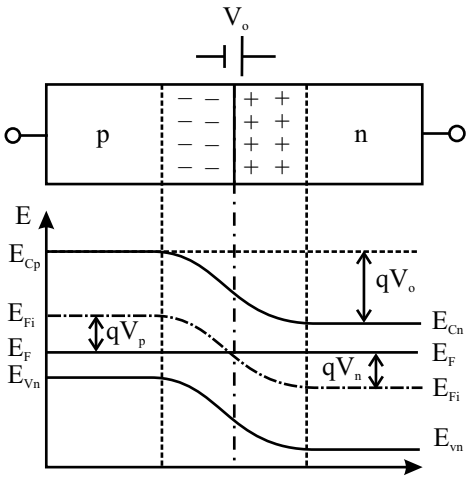


Fig. 2 Energy Band Diagram of Open Circuited pn Junction

The built-in potential at pn junction can be given by,

$$qV_o = q|V_p| + q|V_n|$$

or
$$V_o = |V_p| + |V_n| \quad (2)$$

The concentration of electrons on n-side of the junction is given by,

$$n = N_C e^{-(E_C - E_F)/kT} = n_i e^{(E_F - E_{Fi})/kT} \quad (3)$$

Where, N_C is called density of states in conduction band, k is Boltzmann's constant, T is temperature in kelvin, n_i is intrinsic carrier concentration.

The shift in Fermi-level on n-side of pn function,

$$E_{Fi} - E_F = qV_n$$

$$\Rightarrow \quad n = n_i e^{\frac{qV_n}{kT}}$$

$$\Rightarrow \quad V_n = \frac{kT}{q} \ell n \frac{n}{n_i} \quad (4)$$

For n-side, $n \approx N_D$

$$\therefore \quad V_n = \frac{kT}{q} \ell n \frac{N_D}{n_i} \quad (5)$$

The concentration of holes on p-side of the junction is given by

$$p = N_V e^{-(E_F - E_V) - kT} = n_i e^{(E_{Fi} - E_F)/kT} \quad (6)$$

The shift in Fermi-level on p-side of pn junction,

$$E_{Fi} - E_F = qV_P$$

$$\Rightarrow \quad p = n_i e^{\frac{eV_P}{kT}}$$

$$\Rightarrow \quad V_p = \frac{kT}{q} \ell n \frac{p}{n_i} \tag{7}$$

For p-side, $p \approx N_A$

$$\therefore \quad V_p = \frac{kT}{q} \ell n \frac{N_A}{n_i} \tag{8}$$

Putting expression of V_n and V_p in equation (2), we have,

Built in potential, $$V_o = \frac{kT}{q} \ell n \frac{N_A}{n_i} + \frac{kT}{q} \ell n \frac{N_D}{n_i} = \frac{kT}{q} \ell n \frac{N_A N_D}{n_i^2}$$

$$\Rightarrow \quad \boxed{V_o = V_T \ell n \frac{N_A N_D}{n_i^2}} \tag{9}$$

where $$V_T = \frac{kT}{q} \tag{10}$$

Here V_T has same as of the voltage so it is called Thermal voltage.

2.2.2 Electric Field Intensity of Open Circuited pn Junction

Consider an open circuited pn junction diode is placed along the x-axis with its junction lying at origin as shown in Fig. 3. Let the space charge ends abruptly on p-side at $x = -W_p$ and on n-side at $x = W_n$. The space charge density across the junction can be given as,

$$\rho(x) = -q N_A \quad ; -W_p < x < 0$$
$$= q N_D \quad ; 0 < x < W_n$$

The Poisson's equation of space charge in pn junction can be written as,

$$\frac{d^2V}{dx^2} = -\frac{\rho(x)}{\varepsilon} \tag{11}$$

where V is potential function in depletion region and ε is permitivity of the semiconductor. The electric field in depletion region is related to potential function as,

$$E = -\frac{dV}{dx}$$

$$\Rightarrow \quad \frac{d}{dx}(-E) = -\frac{\rho(x)}{\varepsilon}$$

$$\Rightarrow \quad \frac{dE}{dx} = \frac{\rho(x)}{\varepsilon}$$

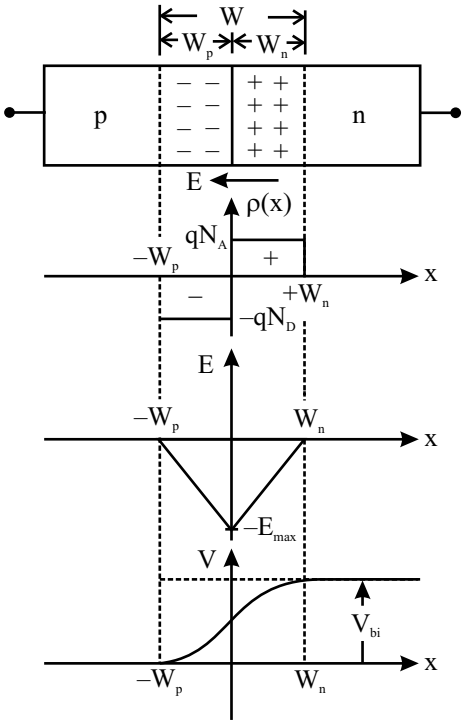


Fig. 3 Variation of ρ, E and V across the depletion region in open circuited pn junction

Case-I : For p-region, $\rho(x) = -q N_A$; $W_p < x < 0$

$$\therefore \quad \frac{dE}{dx} = -\frac{q N_A}{\varepsilon}$$

$$\Rightarrow \quad E = -\int \frac{q N_A}{\varepsilon} dx + C_1 = -\frac{q N_A}{\varepsilon} x + C_1 \qquad (12)$$

Under thermal equilibrium the electric field in n and p regions outside the depletion layer is zero.

$$\therefore \quad E = 0 \text{ at } x = -W_p$$

$$\Rightarrow \quad 0 = -\frac{q N_A}{\varepsilon}\left(-W_p\right) + C_1$$

$$\Rightarrow \quad C_1 = -\frac{q N_A}{\varepsilon} W_p$$

Putting C_1 in equation (12), we have,

$$E = -\frac{q N_A}{\varepsilon}\left(x + W_p\right) \; ; -W_p < x < 0 \qquad (13)$$

Case-II : For n-region, $\rho(x) = q N_D \quad ; \quad 0 < x < W_n$

$$\frac{dE}{dx} = \frac{q N_D}{\varepsilon}$$

$$\Rightarrow \quad E = \int \frac{q N_D}{\varepsilon} dx + C_2 = \frac{q N_D}{\varepsilon} x + C_2 \qquad (14)$$

Applying boundary condition, $E = 0$ at $x = W_n$

$$0 = \frac{q N_D}{\varepsilon} W_n + C_2$$

$$\Rightarrow \quad C_2 = -\frac{q N_A}{\varepsilon} W_n$$

Putting C_2 in equation (14), we have,

$$E = \frac{q N_D}{\varepsilon}(x - W_n) = \frac{q N_D}{\varepsilon} x - \frac{q N_D}{\varepsilon} W_n$$

The variation of electric field as function of x in depletion region is shown in Fig. 3.

The electric field is continuous across the junction and it is maximum at x = 0.

$$\therefore \quad \boxed{E = -\frac{q N_A W_P}{\varepsilon} = -\frac{q N_D W_n}{\varepsilon}} \qquad (15)$$

Note : *The electric field is maximum at the junction for uniformly doped junction.*

2.2.3 Potential Function of Open Circuited pn Junction

The potential function in depletion region of pn function can be obtain using equation of electric field for depletion region.

Case-I : For p-region,

$$E = -\frac{dV}{dx} = -\frac{q N_D}{\varepsilon}(x + W_p) \quad ; \quad -W_p \le x \le 0$$

$$\Rightarrow \quad V = \int \frac{q N_A}{\varepsilon}(x + W_p) dx + C_1'$$

$$\Rightarrow \quad V = \frac{q N_A}{\varepsilon}\left(\frac{x^2}{2} + W_p x\right) + C_1' \qquad (16)$$

Taking $V = 0$ at $x = -W_p$

$$\Rightarrow \quad 0 = \frac{q N_A}{\varepsilon}\left(\frac{W_p^2}{2} - W_p^2\right) + C_1'$$

$$\Rightarrow \qquad C_1' = \frac{q N_A}{2\varepsilon} W_p^2$$

Putting C_1' in equation (16), we have,

$$\therefore \qquad V = \frac{q N_A}{\varepsilon}\left(\frac{x^2}{2} + W_p x\right) + \frac{q N_A}{2\varepsilon} W_p^2$$

$$\Rightarrow \qquad V = \frac{q N_A}{\varepsilon}\left(x + W_p\right)^2 \quad ; \quad -W_p \le x \le 0 \qquad (17)$$

Case-II : For n-region,

$$E = -\frac{dV}{dx} = \frac{q N_D}{\varepsilon}\left(x - W_n\right) \quad ; \quad 0 \le x \le W_n$$

$$\Rightarrow \qquad V = -\int \frac{q N_D}{\varepsilon}\left(x - W_n\right)dx + C_2'$$

$$\Rightarrow \qquad V = \frac{q N_D}{\varepsilon}\left(\frac{-x^2}{2} + W_n x\right) + C_2' \qquad (18)$$

The potential is a continuous function, so equations (17) and (18) give same value of V at $x = 0$.

$$\therefore \qquad C_2' = \frac{q N}{}$$

$$\therefore \qquad V = \frac{q N_D}{2\varepsilon}\left(W_n x - \frac{x^2}{2}\right) + \frac{q N_A}{2\varepsilon} W_p^2 \quad ; \quad 0 \le x \le W_n$$

Potential barrier, $V = V_o$ at $x = W_n$

$$\therefore \qquad V_o = \frac{q N_D}{\varepsilon}\left(W_n^2 - \frac{W_n^2}{2}\right) + \frac{q N_A}{2\varepsilon} W_p$$

$$\boxed{V_o = \frac{q}{2\varepsilon}\left(N_D W_n^2 + N_A W_p^2\right)} \qquad (19)$$

The variation of V as function of x is shown in Fig. 3.

2.2.4 Space Charge or Depletion Layer Width of Open Circuited pn Junction

A semiconductor is always electrical neutral therefore, the magnitude of space charge on n-side of

junction is same as magnitude of space charge on p-side of the junction. Let Q_n is magnitude of space charge on p-side in depletion layer and Q_p is magnitude of space charge as n-side in the depletion layer. Then,

$$Q_n = Q_p$$

$$\Rightarrow \quad qN_A AW_P = q N_D AW_n$$

Where A is cross-section area of the junction.

$$\Rightarrow \quad \boxed{N_A W_p = N_D W_n} \tag{20}$$

Case-I : Space charge width on n-side

Width of depletion layer on n-side of the junction can be given as,

$$W_P = \frac{N_D W_n}{N_A} \tag{21}$$

The built-in potential barrier of the pn junction in terms of depletion layer width is given as,

$$V_o = \frac{q}{2\varepsilon}\left(N_A W_p^{\,2} + N_D W_n^{\,2}\right)$$

$$\Rightarrow \quad V_o = \frac{q}{2\varepsilon}\left(N_A\left(\frac{N_D W_n}{N_A}\right)^2 + N_D W_n^{\,2}\right)$$

$$\Rightarrow \quad \boxed{W_n = \sqrt{\frac{2\varepsilon V_o}{q} \times \frac{N_A}{N_D} \times \frac{1}{N_A + N_D}}} \tag{22}$$

Case-II : Space charge width on p-side

From equation (20), the width of space charge on n-side,

$$W_n = \frac{N_A W_P}{N_D} \tag{23}$$

Built in potential, $$V_o = \frac{q}{2\varepsilon}\left[N_A W_P^{\,2} + N_D\left(\frac{N_A W_P}{N_D}\right)^2\right]$$

$$\Rightarrow \quad \boxed{W_p = \sqrt{\frac{2\varepsilon V_o}{q} \times \frac{N_D}{N_A}\left(\frac{1}{N_A + N_D}\right)}} \tag{24}$$

Total width of the depletion layer,

$$W = W_n + W_p$$

$$W^2 = W_n^2 + 2W_nW_p + W_p^2$$

$$\Rightarrow \quad W = \sqrt{W_n^2 + W_p^2 + 2W_nW_p}$$

Putting the expressions of W_p and W_n from equations (22) and (24) in above relation, we have,

$$\Rightarrow \quad \boxed{W = \sqrt{\frac{2\varepsilon V_o}{q} \times \left(\frac{1}{N_A} + \frac{1}{N_D}\right)}} \qquad (25)$$

Relation between W_p and W:

Total width of depletion region,

$$W = W_n + W_p$$

$$\Rightarrow \quad W_n = W - W_p \qquad (26)$$

Putting expression of W_n from equation (23) in above equation, we have,

$$\frac{N_A}{N_D} W_p = W - W_p$$

$$\Rightarrow \quad \boxed{W_p = \frac{N_D}{N_A + N_D} W} \qquad (27)$$

Relation between W_p and W:

Putting expression of W_p from equation (23) in equation (26), we have,

$$W_n = W - \frac{N_D W_n}{N_A}$$

$$\Rightarrow \quad \boxed{W_n = \frac{N_A}{N_A + N_D} W} \qquad (28)$$

Example 1

Common Data for (i) and (ii)

Consider a Silicon p-n junction at room temperature having the following parameters

Doping on the n-side = 1×10^{17} cm^{-3}

Depletion width on the n-side = 0.1μm

Depletion width on p-side = 1.0 μm

Intrinsic carrier concentration = 1.4×10^{10} cm^{-3}

Thermal voltage = 26 mV

Permitivity of free space = 8.85×10^{-12} $F.cm^{-1}$

Dielectric Constant of Silicon = 12

(i) The built-in potential of the junction

(a) is 0.70 V (b) is 0.76 V

(c) is 0.82 V (d) cannot be estimated from the data given

(ii). The peak electric field in the device is

(a) 0.15 MV · cm^{-1}, directed from p-region to n-region

(b) 0.15 MV · cm^{-1}, directed from n-region to p-region

(c) 1.80 MV · cm^{-1}, directed from p-region to n-region

(d) 1.80 MV · cm^{-1}, directed from n-region to p-region

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Solution

(i) Ans.(b)

The built-in potential of the pn junction is given by,

$$V_o = V_T \ell n \frac{N_D N_A}{n_i^2} \quad \text{.....(i)}$$

Given,

Doping on the n-side,

$$N_D = 1\times10^{17}\ cm^{-3}$$

Depletion width on the n-side,

$$W_n = 0.1\mu m = 0.1\times10^{-4} cm$$

Depletion width on p-side,

$$W_p = 1.0\ \mu m = 1.0\times10^{-4} cm$$

Intrinsic carrier concentration,

$$n_i = 1.4\times10^{10}\ cm^{-3}$$

Thermal voltage, $V_T = 26$ mV

Permitivity of free space, $\varepsilon_o = 8.85\times10^{-14}$ F-cm^{-1}

Dielectric Constant of Silicon $\varepsilon_r = 12$

Relation between depletion layer width on n-side and p-side of junction is given by,

$$W_n N_D = W_p N_A$$

$$\Rightarrow \quad N_A = \frac{W_n N_D}{W_p} = \frac{1\times10^{17}\times0.1\times10^{-4}}{1\times10^{-4}} = 1\times10^{16}\ cm^{-3}$$

Then built-in potential of junction,

$$V_o = 26 \ell n \frac{10^{17}\times10^{16}}{(1.4\times10^{10})^2}\ \text{mV} = 0.76\ \text{V}$$

(ii). Ans.(b)

In a pn junction diode n-side of depletion layer has positive bound charges and p-side has negative bound charges. So electric field is directed from n-side to p-side of junction.

The peak electric field in the depletion layer of device is given by,

$$E_o = \frac{q}{\varepsilon_o \varepsilon_r} N_D W_n$$

$$\Rightarrow \quad E_o = \frac{1.6\times10^{-19}}{8.85\times10^{-14}\times12}\times10^{17}\times0.1\times10^{-6} = 0.15 \text{ MV} \cdot \text{cm}^{-1}$$

Example 2

The donor and accepter impurities in an abrupt junction silicon diode are 1×10^{16} cm^{-3} and 5×10^{18} cm^{-3}, respectively. Assume that the intrinsic carrier concentration is silicon $n_i = 1.5 \times 10^{10}$ cm^{-3} at 300 K, $\frac{kT}{q} = 26$ mV and the permittivity of silicon $\varepsilon_{si} = 1.04 \times 10^{-12}$ F/cm. The built-in potential and the depletion width of the diode under thermal equilibrium conditions, respectively, are

(a) 0.7 V and 1×10^{-4} cm
(b) 0.86 V and 1×10^{-4} cm
(c) 0.7 V and 3.3×10^{-5} cm
(d) 0.86 V and 3.3×10^{-5} cm

GATE(EC-III/2014/2M)

Solution : Ans (d)

The built-in potential of the pn junction under thermal equilibrium is given by,

$$V_o = \frac{kT}{q} \ell n \frac{N_D N_A}{n_i^2} \qquad \text{.....(i)}$$

Given, $N_D = 1 \times 10^{16}$ cm^{-3}

$N_A = 5 \times 10^{18}$ cm^{-3}

$n_i = 1.5 \times 10^{10}$ cm^{-3}

$$\Rightarrow \quad V_o = 26 \ell n \frac{10^{16}\times5\times10^{18}}{(1.5\times10^{10})^2} \text{mV}$$

$$\Rightarrow \quad V_o = 0.86 \text{ V}$$

The depletion layer width of the diode is given by,

$$W = \sqrt{\frac{2\varepsilon V_o}{q}\left(\frac{1}{N_D}+\frac{1}{N_A}\right)}$$

$$\Rightarrow \quad W = \sqrt{\frac{2\times1.04\times10^{-12}\times0.86}{1.6\times10^{-19}}\left(\frac{10^{16}+5\times10^{18}}{10^{16}\times5\times10^{18}}\right)} = 3.3 \times 10^{-5} \text{ cm}$$

Example 3

Consider a silicon *p-n* junction with a uniform acceptor doping concentration of 10^{17} cm^{-3} on the

p-side and a uniform donor doping concentration of 10^{16} cm^{-3} on the *n*-side. No external voltage is applied to the diode. Given: $\frac{kT}{q} = 26$ mV, $n_i = 1.5 \times 10^{10}$ cm^{-3}, $\varepsilon_{Si} = 12\ \varepsilon_0$, $\varepsilon_0 = 8.85 \times 10^{-14}$ F/m, and $q = 1.6 \times 10^{-19}$ C.

The charge per unit junction area (nCcm^{-2}) in the depletion region on the p-side is .....

GATE(EC-I/2016/2M)

Solution: Ans.(–5.0:–4.6)

Given,

$N_A = 10^{17}$ cm^{-3}, $N_D = 10^{16}$ cm^{-3}, $n_i = 1.5 \times 10^{10}$ cm^{-3}, $\frac{kT}{q} = 26$ mV, $\varepsilon_{Si} = 12\ \varepsilon_0$,

$\varepsilon_0 = 8.85 \times 10^{-14}$ F/m or $\varepsilon_0 = 8.85 \times 10^{-16}$ F/c.m.

The built-in potential of the pn junction under thermal equilibrium is given by,

$$V_o = \frac{kT}{q} \ell n \frac{N_D N_A}{n_i^2}$$

$$\Rightarrow \quad V_o = 26 \ell n \frac{10^{16} \times 10^{17}}{(1.5 \times 10^{10})^2} \text{mV}$$

$$\Rightarrow \quad V_o = 0.76 \text{ V}$$

The depletion layer width of the diode is given by,

$$W = \sqrt{\frac{2\varepsilon V_o}{q}\left(\frac{1}{N_D} + \frac{1}{N_A}\right)}$$

$$\Rightarrow \quad W = \sqrt{\frac{2 \times 12 \times 8.85 \times 10^{-16} \times 0.76}{1.6 \times 10^{-19}}\left(\frac{10^{16} + 10^{17}}{10^{16} \times 10^{17}}\right)} = 3.33 \times 10^{-6} \text{ cm}$$

Depletion layer width on n-side,

$$\Rightarrow \quad W_p = \frac{N_D}{N_A + N_D} \times W = \frac{10^{16}}{(10^{16} + 10^{17})} \times 3.33 \times 10^{-6}$$

$$\Rightarrow \quad W_p = 3.02 \times 10^{-7} \text{ cm}$$

The charge in the depletion region on the p-side of junction of area (A) can be given by,

$$Q = -eAN_A W_p$$

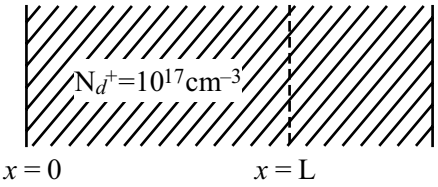
The charge per unit junction area will be,

$$\Rightarrow \quad Q/A = -1.6 \times 10^{-19} \times 10^{17} \times 3.02 \times 10^{-7} \text{ C/cm}^2 = -4.83\ n\text{C/cm}^2$$

Example 4

Consider a region of silicon devoid of electrons and holes, with an ionized donor density of $N_d^+ = 10^{17}$cm^{-3}. The electric field at $x = 0$ is 0 V/cm and the electric field at $x = L$ is 50 kV/cm in the

positive x direction. Assume that the electric field is zero in the y and z directions at all points.



Given $q = 1.6 \times 10^{-19}$ coulomb, $\in_0 = 8.85 \times 10^{-14}$ F/cm, $\in_r = 11.7$ for silicon, the value of L in nm is .....

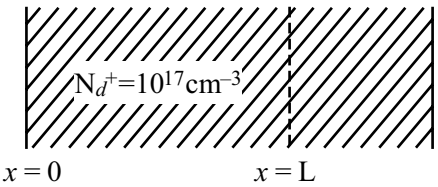
GATE(EC-II/2016/2M)

***Solution :* Ans. (30 to 34)**

The Possion's equation for volume charge distribution inside a semiconductor is given by,

$$\frac{d^2V}{dx^2} = \frac{-\rho}{\varepsilon}$$

when ρ is charge density and ε is permitivity of the semiconductor material.



The electric field is related to the potential field as,

$$E = -\frac{dV}{dx}$$

$$\Rightarrow \quad \frac{d(-E)}{dx} = \frac{-\rho}{\varepsilon_o \varepsilon_r}$$

For ionized donor impurity,

$$\rho = q\, N_D^+$$

$$\Rightarrow \quad \frac{dE}{dx} = \frac{q\, N_D^+}{\varepsilon_o \varepsilon_r}$$

Integrating, above equation, we have,

$$\Rightarrow \quad E = \int \frac{q\, N_D^+}{\varepsilon_o \varepsilon_r} dx + C_1$$

$$\Rightarrow \quad E = \frac{q\, N_D^+}{\varepsilon_o \varepsilon_r} x + C_1$$

Given, $|E| = 0$ at $x = 0$

$\therefore \quad C_1 = 0$

And $|E| = 50$ kV/cm at $x = L$

$$\Rightarrow \quad 50\times10^{3} = \frac{q N_D^{+}}{\varepsilon_o \varepsilon_r} L$$

$$\Rightarrow \quad L = \frac{\varepsilon_o \varepsilon_r}{q N_D^{+}} \times 50\times10^{3}$$

Given $q = 1.6 \times 10^{-19}$ coulomb, $\varepsilon^0 = 8.85 \times 10^{-14}$ F/cm, $\varepsilon_r = 11.7$ for silicon, $N_d^{+} = 10^{17}cm^{-3}$

$$\Rightarrow \quad L = \frac{8.85\times10^{-14}\times11.7}{1.6\times10^{-19}\times10^{17}} \times 50\times10^{3}$$

$$\Rightarrow \quad L = 3.235 \times 10\text{–}6 \text{ cm} = 32.35 \text{ nm}$$

2.3 Reverse Biased pn Junction

A pn junction is revere biased when p-side is connected to negative terminal and n-side is connected to positive terminal of the battery. In a reverse biased mode the negative terminal attracts holes from p-region and positive terminal attracts electrons from n-side and concentration of holes on n-side and electrons on p-side becomes zero at the edges of depletion region on both sides of the junction. Thus concentration of minority carriers becomes zero at edges of the depletion region on both sides as shown in Fig.4. The width of depletion region increases and the potential barrier at the junction is also increased.

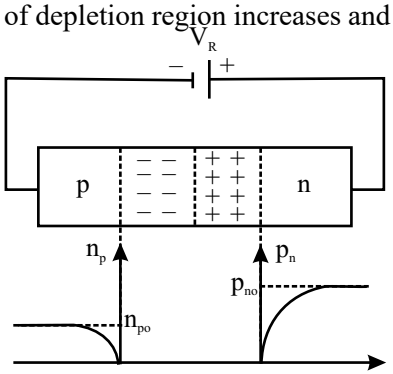


Fig. 4 Variation of minority carrier concentration in reverse biased pn junction

2.3.1 Energy Band Diagram and Space Charge Width in Reverse Biased pn Junction

When a pn junction is reverse biased the Fermi levels on n-side and p-side of the junction is no longer at the same level like open circuited pn junction. The Fermi level on p-side shifts upward and Fermi level on n-side shifts downward. The difference in Fermi levels on p-side and n-side of the junction is qV_R where V_R is reverse bias voltage. The potential barrier across the junction is raised from V_o to $V_o + V_R$. Thus for crossing of the junction an electron needs to overcome potential barrier which is sum of built-in potential and reverse bias voltage.

So, the total potential barrier under reverse biased pn junction becomes,

$$V_j = V_o + V_R$$

The energy band diagram of a reverse biased pn junction is as shown in Fig. 5.

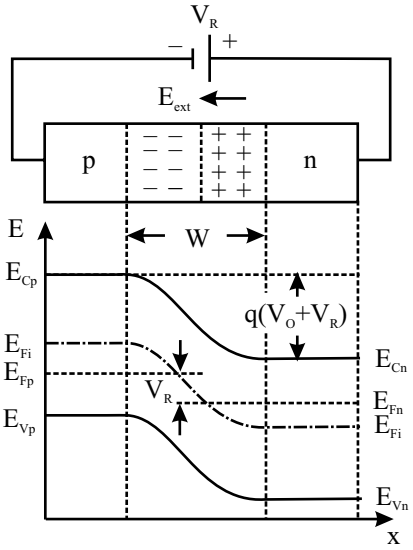


Fig. 5 Energy band diagram of reverse biased pn junction

Then total width of depletion layer under reverse biased condition can be obtained by replacing V_o by $V_o + V_R$ in equation (25) as under,

$$W = \sqrt{\frac{2\varepsilon(V_o + V_R)}{q} \times \left(\frac{1}{N_A} + \frac{1}{N_D}\right)} \tag{29}$$

2.3.2 Electric Field in Reverse Biased pn Junction

When the pn junction is reverse biased the depletion region has two components of field one component is due to space charge of depletion layer and another component is induced field due to external reverse biasing voltage. The external component results in additional bound charges stored in depletion layer which is possible only if width of the depletion layer is increased. The electric field in depletion region still remains linear function and is maximum at metallurgical junction. The maximum electric field at junction is given by equation (15), however, it is with increased width of depletion layers on n and p sides.

$$E_{max} = -\frac{q N_D W_n}{\varepsilon} = -\frac{q N_A W_p}{\varepsilon} \tag{30}$$

The width of depletion layers on n-side & p-side for reverse biased pn junction can be obtained by replacing V_o by $V_o + V_R$ in equation (22) & (24) as under,

$$W_n = \sqrt{\frac{2\varepsilon(V_o + V_R)}{q} \frac{N_A}{N_D} \times \frac{1}{N_A + N_D}} \tag{31}$$

and $$W_p = \sqrt{\frac{2\varepsilon(V_o + V_R)}{q} \cdot \frac{N_D}{N_A} \cdot \frac{1}{N_A + N_D}} \quad (32)$$

$$\Rightarrow \quad E_{max} = -\frac{q N_D}{\varepsilon} \times \sqrt{\frac{2\varepsilon(V_o + V_R)}{q} \cdot \frac{N_A}{N_D} \cdot \frac{1}{N_A + N_D}}$$

$$\Rightarrow \quad E_{max} = -\sqrt{\frac{2q}{\varepsilon}(V_o + V_R)\frac{N_A N_D}{N_A + N_D}} \quad (33)$$

From (29) and (33), we have,

$$E_{max} = -\frac{2(V_o + V_R)}{W} \quad (34)$$

2.4 Forward Biased pn Junction

A pn junction is forward biased when p-side is connected to positive terminal and n-side is connected to negative terminal of the battery. The electric field induced due to forward biased voltage opposes the internal electric field of depletion layer and thus net field in the depletion region is reduced. The reduction in electric field due forward biased voltage reduces the space charge stored in the depletion layer and hence potential barrier and the width of depletion layer is reduced. However, the electric field is zero in p ad n layers beyond the boundaries of depletion layer.

2.4.1 Energy Band Diagram and Space Charge Width in Forward Biased pn Junction

When a pn junction is forward biased the Fermi level on p-side shifts down ward downward and Fermi level on n-side shifts upward. The difference in Fermi levels on p-side and n-side of the junction is qV_F where V_F is forward bias voltage. The potential barrier across the junction is reduced from V_o to $V_o - V_F$.

So, the total potential barrier under forward biased pn junction becomes,

$$V_j = V_o - V_F$$

The energy band diagram of a reverse biased pn junction is as shown in Fig. 6.

Then total width of depletion layer under reverse biased condition can be obtained by replacing V_o by $V_o - V_F$ in equation (25) as under,

$$\boxed{W = \sqrt{\frac{2\varepsilon(V_o - V_F)}{q} \times \left(\frac{1}{N_A} + \frac{1}{N_D}\right)}} \quad (35)$$

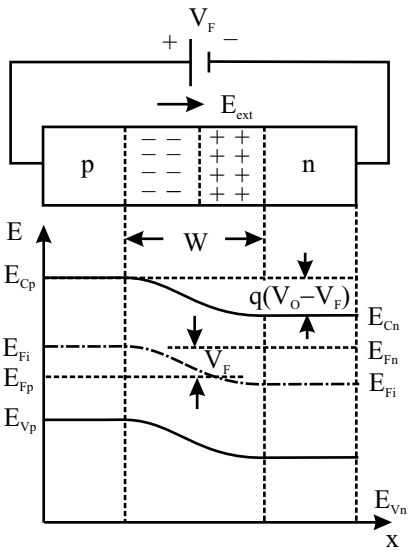


Fig. 6 Energy band diagram of forward biased pn junction

2.4.2 Carrier Concentrations in Forward Biased pn Junction

In a forward biased pn junction the negative terminal of the battery repels electrons from n-region and positive terminal repels holes from p-region towards the junction. The the holes are injected from p-side to n-side and electrons are injected from n-side to p-side across the junction. The concentration of the electrons on p-side at the edge of depletion layer is $p_n(W_n)$ and concentration of holes on n-side at edge of depletion layer is $n_p(-W_p)$. The concentration of minority carriers reduces exponentially through p and n layers and settles to a value equal to thermal equilibrium value of p_{no} and n_{po} as shown in the Fig. 7. The concentrations of minority carriers is maximum at edges of depletion layer. The concentrations of majority carriers reduces exponentially from their thermal equilibrium values (i.e.n_{no} &p_{po}) near junction area due to increased recombination with minority carriers.

The potential barrier of pn junction under thermal equilibrium when no bias voltage is applied is given by,

$$V_o = \frac{kT}{q}\ell n\frac{N_A N_D}{n_i^2} = V_T \ln\frac{N_A N_D}{n_i^2}$$

If we assume complete ionization of acceptor impurities at thermal equilibrium then acceptor concentration, $N_A \approx p_{po}$

And $\frac{n_i^2}{N_D} \approx p_{no}$

Where, p_{po} is concentration of holes on p-side and p_{no} is concentration of holes on n-side at thermal equilibrium.

$$\Rightarrow \quad V_o = \frac{kT}{q}\ell n\frac{p_{po}}{p_{no}} = V_T \ln\frac{p_{po}}{p_{no}} \qquad (36)$$

$$\Rightarrow \quad p_{no} = p_{po} e^{-\frac{qV_o}{kT}} = p_{po} e^{-\frac{V_o}{V_T}} \tag{37}$$

Similarly, if we assume complete ionization of donor impurities, the concentration of electrons on n-side under thermal equilibrium,

$n_{no} = N_D$

And concentration of electrons an p-side under thermal equilibrium,

$$n_{po} \approx \frac{n_i^2}{N_A}$$

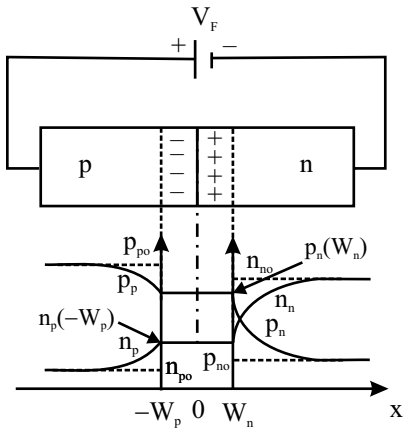


Fig. 7 Variation of carrier concentration in forward biased pn junction

Then potential barrier can be written as,

$$V_o = \frac{kT}{q} \ell n \frac{n_{no}}{n_{po}} = V_T \ln \frac{n_{no}}{n_{po}} \tag{38}$$

$$\Rightarrow \quad n_{po} = n_{no} e^{-\frac{qV_o}{kT}} = n_{no} e^{-\frac{V_o}{V_T}} \tag{39}$$

For a forward biased p-n junction the effective potential barrier changes from V_o to $V_o - V_F$.

So, voltage V_o in equation (39) is replaced by $V_o - V_F$ to get concentration of electrons on p-side at the edge of depletion layer. Under forward biased conditions at low level injection, the majority carrier concentration remains almost same as at thermal equilibrium i.e. $n_{no} \approx n_n$ and $p_{po} \approx p_p$. However, the minority carrier concentration at the edge of depletion layer changes from n_{po} to $n_p(-W_p)$ on p-side and from p_{no} to $p_n(W_n)$. Then equation (37) for a forward biased junction can be written as,

$$p_n(W_n) = p_{po} e^{\frac{-q(V_o - V_F)}{kT}} = p_{po} e^{\frac{-qV_o}{kT}} \cdot e^{\frac{qV_F}{kT}}$$

$$\Rightarrow \quad \boxed{p_n(W_n) = p_{no} e^{\frac{qV_F}{kT}} = p_{no} e^{\frac{V_F}{V_T}}} \tag{40}$$

Thus concentration of holes at edge of depletion layer on n-side is increase from p_{no} to p_n when the

junction is forward biased.

Similarly, the concentration of electrons at edge of depletion layer on n-side under forward biased mode can be written as under,

$$\boxed{n_p(-W_p) = n_{po} e^{\frac{qV_F}{kT}} = n_{po} e^{\frac{V_F}{V_T}}} \quad (41)$$

The equation (40) and (41) are called laws of junction.

The minority carriers on n-side and p-side of the junctions diffuses through the n and p layers due to the concentration gradient on minority carriers. The concentrations of minority carriers as function of distance on both sides of the junction can be obtained using concept of diffusion of carriers as under,

$$p_n(x) = p_{no} - (p_{no} - p_n(W_n))\, e^{-\frac{x-W_n}{L_p}} \quad (42)$$

Similarly concentration of electrons on p-side can be given as,

$$n_p(x) = n_{po} - (n_{po} - n_p(-W_p))\, e^{\frac{x+W_p}{L_p}} \quad (43)$$

The excess minority carriers injected on p and n-sides of the junction under forward biased condition can be given by,

$$\delta p_n(x) = p_n(x) - p_{no} = (p_n(W_n) - p_{no})\, e^{-\frac{x-W_n}{L_p}} = \delta p_n(W_n)\, e^{-\frac{x-W_n}{L_p}} \quad (44)$$

$$\delta n_p(x) = n_p(x) - n_{po} = (n_p(-W_p) - n_{po})\, e^{\frac{x+W_p}{L_p}} = \Delta n_p(-W_p)\, e^{\frac{x+W_p}{L_p}} \quad (45)$$

The excess minority injected on p and n-sides of the junction at the edge of the junction under forward biased condition are given by,

$$\delta p_n = p_n(W_n) - p_{no} = p_{no}(e^{\frac{qV_F}{kT}} - 1) = p_{po}(e^{\frac{V_o}{V_T}} - 1) \quad (46)$$

And

$$\delta n_p = n_p(-W_p) - n_{po} = n_{po}(e^{\frac{qV_P}{kT}} - 1) = \quad (47)$$

2.5. Generalized Expression of Depletion Layer Width of pn Junctions and Unipolar Junctions

Total width of depletion layer changes with the biasing voltage depending upon the type of biasing. The generalized expression of width of depletion layer as a function of biasing voltage can be given as

$$W = \sqrt{\frac{2\varepsilon}{q}\left[\frac{1}{N_A}+\frac{1}{N_D}\right]V_j} \quad (48)$$

Where, V_j is effective potential barrier at the junction.

$V_j = V_o$; For an open circuited pn junction

$V_j = V_o + V_R$; For a reverse biased pn junction

$V_j = V_o - V_F$; For a forward biased pn junction

Note : *i. Width of the depletion layer increases with reverse biasing and reduces with forward biasing.*

ii. With increase in the concentration of the impurities the width of the depletion region decreases.

Case-I : When p-side is heavily doped as compared to n-side i.e. $N_A >> N_D$

$$\Rightarrow \quad \frac{1}{N_A} << \frac{1}{N_D}$$

$$\Rightarrow \quad \frac{1}{N_A}+\frac{1}{N_D} \approx \frac{1}{N_D}$$

Width depletion layer, $W \approx W_n \approx \sqrt{\frac{2\in}{q}\left[\frac{1}{N_D}\right]V_j}$ (49)

Thus most of the depletion layer lies on n-side of the junction when p-side is heavily doped as compared to the n-side.

Case-II : When n-side is heavily doped as compared to p-side i.e. $N_D >> N_A$

Then, $$\frac{1}{N_D} << \frac{1}{N_A}$$

$$\therefore \quad \frac{1}{N_A}+\frac{1}{N_D} \approx \frac{1}{N_A}$$

Width depletion layer, $W \approx W_P \approx \sqrt{\frac{2\in}{q}\left[\frac{1}{N_A}\right].V_j}$ (50)

Thus most of the depletion layer lies on p-side of the junction when n-side is heavily doped as compared to the p-side.

When most of depletion layer lies on one side of the pn junction then such type of junctions are called one sided. The variation of charge density, electric field and potential across a one sided junction with heavily doped p-side as compared to n-side is as shown in Fig. 8

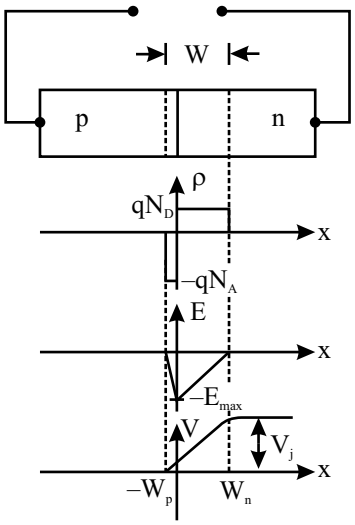


Fig.8 Variation of ρ, E and V across a one sided junction

Note : *When a junction is one sided the expression of electric field remains same as open circuited pn junction as under,*

$$E_{max} = -\frac{q N_D W_n}{\varepsilon} = -\frac{q N_A W_p}{\varepsilon} \qquad (51)$$

Note : *Built-in potential of Unipolar Junctions*

The unipolar junctions are the junctions with similar type doping on both side of junction with varying impurity concentration across the junction. The built-in potential of these junction is given as follows,

i. The built-in potential of unipolar n^+-n junction is given by,

$$V_o = \frac{kT}{q} \ell n \frac{N_D^+}{N_D}$$

ii. The built-in potential of unipolar n^--n junction is given by,

$$V_o = \frac{kT}{q} \ell n \frac{N_D}{N_D^-}$$

iii. The built-in potential of unipolar p^+-p junction is given by,

$$V_o = \frac{kT}{q} \ell n \frac{N_A^+}{N_A}$$

iv. The built-in potential of unipolar p^--p junction is given by,

$$V_o = \frac{kT}{q} \ell n \frac{N_A}{N_A^-}$$

It should be observed that the higher concentration of impurity is taken in numerator and lower

concentration in denominator in the expression of built-in potential of unipolar semiconductor junctions.

Example 5

A p^+ n junction has a built-in potential of 0.8 V. The depletion layer width at a reverse bias of 1.2 V is 2 μm. For a reverse bias of 7.2 V, the depletion layer width will be

(a) 4 μm (b) 4.9 μm

(c) 8 μm (d) 12 μm

GATE(EC/2007/2M)

Solution: Ans.(a)

The width of depletion layer,

$$W \propto V_j^{+m}$$

where, $m = 1/2$; for step graded or abrupt junction

$= 1/3$; for linearly graded junction

$V_j = V_0$; for no biasing voltage

$= V_0 - V_F$; For forward biased

$= V_0 + V_R$; For reverse biased

V_0 = Barrier potential

V_R = reverse biasing voltage

V_F = forward biasing voltage

Assuming, abrupt junction , we have,

$$W \propto (V_0 + V_R)^{+1/2}$$

$$\Rightarrow \quad \frac{W_2}{W_1} = \left(\frac{V_o + V_{R2}}{V_o + V_{R1}}\right)^{1/2}$$

$$\Rightarrow \quad W_2 = \left(\frac{V_o + V_{R2}}{V_o + V_{R1}}\right)^{1/2} \times W_1,$$

$$\Rightarrow \quad W_2 = \frac{(0.8+7.2)^{+1/2}}{(0.8+1.2)^{+1/2}} \times 2\ \mu m = 4\ \mu m$$

Example 6

A junction is made between p^- Si with doping density $N_{A1} = 10^{15}$ cm^{-3} and p Si with doping density $N_{A2} = 10^{17}$ cm^{-3}.

Given : Boltzmann constant k = 1.38 ×10^{-23} J.K^{-1}, electronic charge q = 1.6 ×10^{-19} C. Assume 100% acceptor ionization. At room temperature (T = 300K), the magnitude of the built-in potential (in volts, correct to two decimal places) across this junction will be _____.

GATE(EC/2018/2M)

Solution : Ans.(0.11 to 0.13)

The built-in potential of unipolar p^--p junction is given by,

$$V_o = \frac{kT}{q} \ell n \frac{N_A}{N_A^-}$$

Given, $N_A = N_{A2} = 10^{17}\ cm^{-3}$

$N_A^- = N_{A1} = 10^{15}\ cm^{-3}$

$$\Rightarrow \quad V_o = \frac{1.38\times10^{-23}\times300}{1.6\times10^{-19}} \ell n \frac{10^{17}}{10^{15}}$$

$$\Rightarrow \quad V_o = 0.119\ V$$

2.6. Components of Current in PN Junction Diode

Current in a pn junction diode is contributed by jumping of holes from p-side to n-side, jumping of electrons from n-side to p-side under the influence of external forward biasing voltage and jumping of thermally generated holes from n-side to p-side and jumping of thermally generated electrons from p-side to n-side. The component of current due to crossing of junction by thermally generated minority charge carriers is called reverse saturation current. This component of current is negligible. So, majority of the diode current is due to jumping of holes from p-side to n side and jumping of electrons from n-side to p-side of the junction under the influence of external forward biasing voltage.

2.6.1 Components of Currents in Forward Biased Diode

When a diode is applied with a forward bias voltage, the holes are injected from p-side to n-side and electrons are injected n-side to p-side. The injected electrons from n-side to p-side constitute minority carrier diffusion current (I_{np}). Similarly, the holes are injected from p-side to n-side constitute minority carrier diffusion current on n-side (I_{pn}). The current due to majority carriers on both sides of junction is always a drift current. It is assumed that it is a low level injection where drift current of minority carriers is negligible. It is also observed that at far end away from junction is mostly drift component of current which dominates.

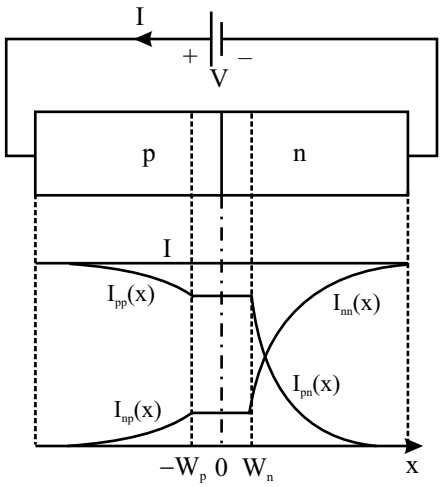


Fig.9 Diode current under forward biased mode

It is also assumed that p-side is heavily doped as compared to n-side. The diffusion current of holes on n-side is denoted by $I_{pn}(x)$ and diffusion current of electrons on p-side is denoted by $I_{np}(x)$. The hole diffusion current density on n-side is given by,

$$J_{pn}(x) = -q D_p \frac{dp_n(x)}{dx}$$

The concentration of holes on n-side with low level injection is given by,

$$p_n(x) = p_{no} - \left(p_{no} - p_n(W_n)\right) e^{-\frac{x-W_n}{L_p}} \tag{52}$$

$$\Rightarrow \quad J_{pn}(x) = q D_p \frac{\left(p_n(W_n) - p_{no}\right)}{L_p} \cdot e^{-\frac{x-W_n}{L_p}} \tag{53}$$

The concentration of holes on n-side at edge of depletion layer can be given by replacing V_F by V in equation (40) as under,

$$p_n(W_n) = p_{no} e^{\frac{qV}{kT}}$$

$$\Rightarrow \quad J_{pn}(x) = \frac{q D_p p_{no}}{L_p} \left(e^{\frac{qV}{kT}} - 1 \right) e^{-\frac{x-W_n}{L_p}} \tag{54}$$

The diffusion current of hole $x = W_n$ on edge of depletion layer on n-side,

$$J_{pn}(W_n) = \frac{q D_p p_{no}}{L_p} \left(e^{\frac{qV}{kT}} - 1 \right) \tag{55}$$

Similarly, the diffusion current density of electron an p-side of junction at edge of depletion layer at $x = -W_p$ can be computed as,

$$J_{np}(-W_p) = \frac{q D_n n_{po}}{L_n} \left(e^{\frac{qV}{kT}} - 1 \right) \tag{56}$$

The electrons and holes at junction cross in the opposite directions but their current is in the same direction. So, total diode current is algebraic sum of electrons and hole diffusion currents at the edge of junction barrier.

$$J = J_{pn}(W_n) + J_{np}(-W_p)$$

$$\Rightarrow \quad J = \left[\frac{q D_p p_{no}}{L_p} + \frac{q D_n n_{po}}{L_n} \right] \left(e^{\frac{qV}{kT}} - 1 \right) \tag{57}$$

The current density in terms of diode current is given by,

$$J = \frac{I}{A}$$

Where A is cross-sectional area of the junction of the diode.

$$\Rightarrow \quad I = \left[\frac{qA D_p p_{no}}{L_p} + \frac{q AD_n n_{po}}{L_n}\right]\left(e^{\frac{qV}{kT}} - 1\right) \tag{58}$$

$$\Rightarrow \quad \boxed{I = I_o\left(e^{\frac{V}{V_T}} - 1\right)} \tag{59}$$

where, $$\boxed{I_o = \frac{Aq D_p p_{no}}{L_p} + \frac{Aq D_n n_{po}}{L_n}} \tag{60}$$

And $$\boxed{V_T = \frac{kT}{q}} \tag{61}$$

Here, I_o is called reverse saturation current of the diode and V_T is called thermal voltage.

The reverse saturation current is purely due to jumping of thermally generated minority carriers across the junction. In other word the reverse saturation current is due to jumping of thermally generated holes from n-side and thermally generated electrons from p-side across the junction.

Majority carrier component of currents in forward biased diode :

Diode current on both the junction is due to both electrons and holes and total current due to electrons and holes at any point is constant and equal to I. The majority carrier drift current an n-side can be given by,

$$I_{nn}(x) = I - I_{pn}(x) = q\mu_n N_D E \tag{62}$$

Similarly, the majority carrier drift current on p-side of junction can be given by,

$$I_{pp}(x) = I - I_{np}(x) = q\mu_p N_A E \tag{63}$$

2.6.2 Components of Currents in Reverse Biased Diode

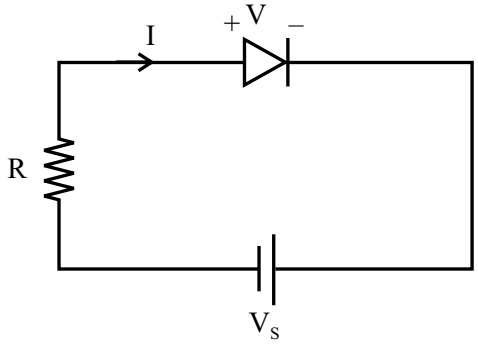


Fig.10 Diode current under reverse biased mode

When diode is reverse biased the current is negligible and whole of the supply voltage appears across the diode,

$$\therefore \quad V = -V_s$$

Then the diode current , $I = I_o(e^{\frac{-V_S}{V_T}} - 1)$

Assuming $V_s >> V_T$ then, $e^{\frac{-V_S}{V_T}} << 1$

$$\Rightarrow \quad I = -I_o \tag{64}$$

Therefore, the current through diode under reverse biased condition is equal to the reverse saturation current.

Note : *1. Reverse saturation current of a diode is independent of biasing voltage.*

2. The reverse saturation current is function of minority carrier concentration which increases with increase in temperature $(n_i \propto T^{\frac{3}{2}})$. *Thus, the reverse saturation current increases with increase in temperature.*

3. The reverse saturation current gets doubled for every 10 °C rise in the junction temperature.

Example 7

At 300 K, for a diode current of 1 mA, a certain germanium diode requires a forward bias of 0.1435 V, whereas a certain silicon diode requires a forward bias of 0.718 V. Under the conditions stated above, the closest approximation of the ratio of reverse saturation current in germanium diode to that in silicon diode is

(a) 1 (b) 5

(c) 4×10^3 (d) 8×10^3

GATE(EC/2003/2M)

Solution: Ans.(c)

The diode current equation is given by

$$I = I_o\left[e^{\frac{V_D}{\eta V_T}} - 1\right]$$

where, V_D = voltage across the diode

$$V_T = \text{Thermal voltage} = \frac{T}{11600}$$

$$\eta = 1 \text{ for Ge}$$

$$= 2 \text{ for Si}$$

The ratio of diode currents for Si and Ge will be,

$$\frac{\text{Si}}{\text{Ge}} = \frac{I_{o,Si}\left[e^{\frac{V_{Si}}{2\times V_T}} - 1\right]}{I_{o,Ge}\left[e^{\frac{V_{Ge}}{1\times V_T}} - 1\right]}$$

Given, $V_{Si} = 0.718$ V, $V_{Ge} = 0.1435$, T = 300 K

At $T = 300$ K,

$$V_T = \frac{300}{11600} = 0.02586$$

$$\Rightarrow \quad \frac{1\times10^{-3}}{1\times10^{-3}} = \frac{I_{o,Si}\left[e^{\frac{0.718}{2\times0.02586}} - 1\right]}{I_{o,Ge}\left[e^{\frac{0.1435}{1\times0.02586}} - 1\right]}$$

$$\Rightarrow \quad \frac{I_{o,Ge}}{I_{o,Si}} = \frac{e^{\frac{0.718}{2\times0.02586}} - 1}{e^{\frac{0.1435}{1\times0.02586}} - 1} = 3993.7 = 4\times10^3$$

The closest approximation is 4×10^3

Example 8

A Silicon PN junction at a temperature of 20°C has a reverse saturation current of 10 pico-Amperes (pA). The reverse saturation current at 40°C for the same bias is approximately

(a) 30 pA (b) 40 pA

(c) 50 pA (d) 60 pA

GATE(EC/2005/1M)

Solution: Ans.(b)

The reverse saturation current as a function of temperature is given by,

$$I_{o2} = I_{o1} \times 2^{\left[\frac{T_2 - T_1}{10}\right]}$$

$$\Rightarrow \quad I_{o2} = I_{o1} \times 2^{(40-20)/10}$$

$$\Rightarrow \quad I_{o2} = I_{o1} \times 2^2 = 4I_{o1}$$

$$\Rightarrow \quad I_{o2} = 4\times10 = 40 \text{ pA}$$

Example 9

For a silicon diode with long P and N regions, the accepter and donor impurity concentrations are 1×10^{17} cm^{-3} and 1×10^{15} cm^{-3}, respectively. The life times of electrons in P region and holes in N region are both 100 μs. The electron and hole diffusion coefficients are 49 cm^2/s and 36 cm^2/s, respectively. Assume $kT/q = 26$ mV, the intrinsic carrier concentration is 1×10^{10} cm^{-3}, and $q = 1.6 \times 10^{-19}$ C. When a forward voltage of 208 mV is applied across the diode, the hole current density (in nA/cm^2) injected from P region to N region is .....

GATE(EC-I/2015/2M)

Solution: Ans.(28 to 30)

Given $q = 1.6 \times 10^{-19}$

Donor concentration , $N_D = 10^{15}\ cm^{-3}$

Acceptor concentration, $N_A = 10^{17}\ cm^{-3}$

$$\frac{kT}{q} = 26\ mV = 26 \times 10^{-3}$$

Average life of electrons and holes

$$\tau_n = \tau_p = 100\ \mu s = 100 \times 10^{-6},$$

Diffusion content of holes, $D_p = 36\ cm^2/s$

Diffusion constant electrons, $D_n = 49\ cm^2/s$

Forward biasing voltage, $V_F = 208 \times 10^{-3}\ V$

Intrinsic carrier concentration, $n_i = 10^{10}\ cm^{-3}$

Concentration of holes on n-side at thermal equilibrium,

$$p_{no} = \frac{n_i^2}{n_n} = \frac{n_i^2}{N_D} = \frac{(10^{10})^2}{(10)^{15}}$$

$$\Rightarrow \quad p_{no} = 10^5\ cm^{-3}$$

Diffusion length of holes,

$$L_p = \sqrt{D_p \tau_p} = \sqrt{36 \times 100 \times 10^{-6}} = 6 \times 10^{-2}\ cm$$

The hole current density due holes injected from p to n side of pn junction diode is given by,

$$J_{pn}(x) = q D_p \frac{dp_n(x)}{dx}$$

Concentration of holes on p-side is given by,

$$p_n(x) = p_{no} - (p_{no} - p_n(0))e^{-\frac{x}{L_p}}$$

Where p_{no} is concentration of holes in base at thermal equilibrium and $p_n(0)$ is concentration of concentration of holes at edge of depletion layer of on n-side and L_p is diffusion length of holes on n-side.

$$\therefore \quad \frac{dp_n(x)}{dx} = \frac{p_{no} - p_n(0)}{L_p} e^{-\frac{x}{L_p}}$$

$$\therefore \quad J_{pn}(x) = -q D_p \frac{(p_{no} - p_n(0))}{L_p} e^{-\frac{x}{L_p}}$$

Injected current at junction at x = 0,

$$J_{pn}(0) = qD_p \frac{(p_n(0) - p_{no})}{L_p}$$

The concentration of holes at the junction in terms of forward forward biasing voltage biasing voltage is given by,

$$p_n(0) = p_{no}\, e^{-\frac{qV_F}{kT}}$$

$$\therefore \quad J_{pn}(0) = \frac{qD_p p_{no}}{L_p}\left(e^{-\frac{qV_F}{kT}} - 1\right)$$

$$\Rightarrow \quad J_{pn}(0) = \frac{1.6\times10^{-10}\times36\times10^{5}\left(e^{\frac{208}{26}} - 1\right)}{6\times10^{-2}} = 28.61 \text{ nA/cm}^2$$

2.7 Characteristics of PN Junction Diode

2.7.1 V-I Characteristic

The VI characteristics of a pn junction diode are shown in Fig.11. When the diode is forward biased the current in the diode is almost zero until the voltage across the diode becomes equal to a critical value called cut-in or offset or break-in or threshold voltage (V_γ). The cut-in voltage is approximately 0.2 V for Ge and 0.6 V for Si. When forward bias voltage becomes more than the cut-in voltage the diode current increases exponentially. The current through the diode under forward biased condition is given by,

$$\boxed{I = I_o(e^{\frac{V_D}{\eta V_T}} - 1)} \qquad (65)$$

Where, η is called ideality factor. η is 1 for Ge and 2 for Si at rated current.

At low current the forward biasing voltage results in reduction of potential barrier of the diode and change of current is small. However, at larger current the diode characteristics becomes almost linear due to resistance offered by p and n layers of the diode.

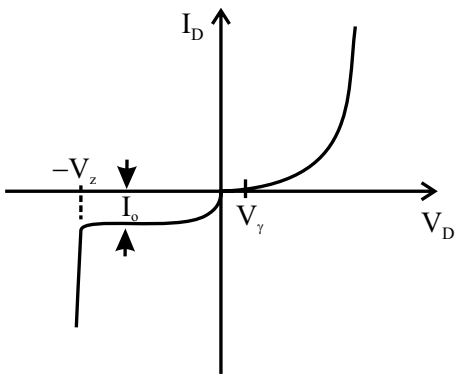


Fig.11 V-I characteristics of pn diode

Note : $V_\gamma = 0.2V$; for Ge

$= 0.6V$; for Si

When the diode is reverse biased with reverse voltage several times the thermal voltage (V_T), the current is negligible through the diode. This current is equal to the reverse saturation current (I_o) of the diode. When the reverse biasing voltage crosses certain critical value called Zener voltage (V_z), there is generation of large number of electron hole pairs in depletion region resulting into a breakdown of junction called Zener breakdown, and a large current starts flowing through the diode in reverse direction from n -side to p-side. This region of the VI characteristics of the diode is *breakdown* region. Under reverse biased condition the voltage across the diode becomes V_z and current through the diode is governed by resistance of the external circuit.

Note : *The diode behaves like an open circuit under reverse biased condition before breakdown. Resistance of a diode in a reverse biased mode is of order of Mega-ohms.*

Note : *Reverse saturation current is of order of micro-amperes for Ge and it is of order of nano-amperes for Si diode.*

2.7.2 Temperature Dependence of V-I characteristic of pn junction diode

a) Variation of voltage across diode under forward bias with temperature

When temperature of a diode is increased, the electron-hole, pairs are generated resulting into reduction in resistance of the diode hence the voltage drop across the diode, under the forward biased condition. Thus the voltage drop across the forward bias diode reduces with increase in temperature. The rate of change of voltage as a function of temperature under the forward biased diode condition is given by,

$$\boxed{\frac{\partial V_D}{\partial T} = -2.5 \text{ mV}/^oC} \quad ; \text{ For both Si and Ge.} \tag{66}$$

b) Variation of reverse saturation current with temperature

When temperature of reverse biased pn junction diode is increased there is generation of electron hole pairs. These additionally generated electron-holes pairs jump across the junction and result in increase in reverse saturation current of the diode. The reverse saturation current doubles for every 10°C rise in temperature in both Si and Ge. The reverse saturation current as a function of temperature is governed by the following relation,

$$\boxed{I_{oT} = I_{oT_1}\, 2^{\left(\frac{T - T_1}{10}\right)}} \tag{67}$$

Note : *Theoretically,the reverse saturation current increases by 8 percent/°C for Si and 11 percent /°C for Ge but experimentally it increases by 7 percent /°C rises in temperature for both Ge and Si.*

2.7.3 Logarithmic Characteristic

The logarithmic characteristics of the diode are applicable for small value of the diode current. Current through a diode under forward biased condition is given by

$$I_D = I_o[e^{\frac{V_D}{\eta V_T}} - 1]$$

When the forward biasing voltage of the diode is several times of thermal voltage the diode current can be taken approximately as under,

$$\Rightarrow \quad I_D = I_o e^{\frac{V_D}{\eta V_T}} - I_o \approx I_o e^{\frac{V_D}{\eta V_T}}$$

$$\Rightarrow \quad I_D = I_o e^{\frac{V_D}{\eta V_T}}$$

Taking natural log on both sides, we have,

$$\ell n\, I_D = \ell n\, I_o + \ell n\, e^{\frac{V_D}{\eta V_T}}$$

$$\Rightarrow \quad \ell n\, I_D = \frac{1}{\eta V_T} . V_D + \ell n\, I_o \qquad (68)$$

If $\ell n I_D$ is taken as y-axis and V_D as x-axis then above equation represents an equation of a straight line which is drawn in Fig.11. Thus, the logarithmic characteristics of a diode are linear.

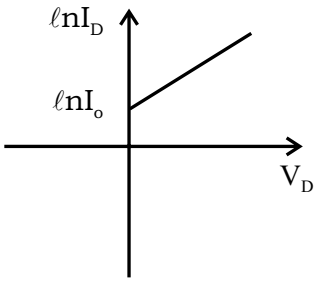


Fig.12 Logarithmic characteristic of a diode

Note : *Logarithmic characteristic of a diode is a linear characteristic. It is applicable for small signal analysis of diode.*

2.7.4 Piecewise linear characteristic

Piece wise linear characteristic of diode is applicable for large signal**.** For large signals the V–I characteristics, of a diode is almost linear as shown in Fig.13.

The inverse of slope of piecewise linear characteristic is called forward resistance of diode at large signals.

Mathematically, the forward resistance of diode for large signals is given by,

$$R_f = \frac{d V_D}{d I_D} \quad ; \text{ for } V_D > V_r \qquad (69)$$

$$= \infty \quad ; \text{ for } V_D < V_r$$

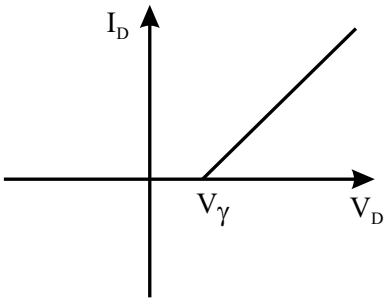


Fig.13 Piecewise linear characteristics of a diode

Example 10

A silicon PN junction is forward biased with a constant current at room temperature. When the temperature is increased by 10°C, the forward bias voltage across the PN junction.

(a) increases by 60 mV (b) decreases by 60 mV

(c) increases by 25 mV (d) decreases by 25 mV

GATE(EC/2011/1M)

Solution: Ans.(d)

The voltage drop across a forward bias junction reduces at the rate of –2.5 mV/°C.

So, $\frac{dV_D}{dT} = -2.5 \text{ mV/°C}$

$\Rightarrow$ $dV_D = -2.5\, dT$

Given, $dT = 10°C$

$\Rightarrow$ $dV_D = -25 \text{ mV}$

So forward voltage across diode decreases by 25 mV when temperature is increased by 10°C.

Example 11

A forward-biased silicon diode when carrying negligible current, has a voltage drop of 0.64 V. When the current is 1A it dissipates 1 W. The ON resistance of the diode is

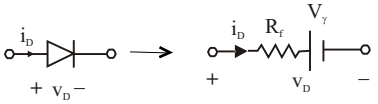
(a) 0.36 Ω (b) 0.64 Ω

(c) 0.72 Ω (d) 1.0 Ω

GATE(IN/2003/2M)

Solution: Ans.(a)

The piecewise linear model of diode is as shown below,



Here, R_f = ON state resistance of diode

and V_γ = cut-in voltage of diode

The power dissipated in diode is given by,

$$P = v_D i_D = V_\gamma i_D + i_D^2 R_f$$

$$\Rightarrow \quad 1 = 0.64(1) + (1)^2 R_f$$

$$\Rightarrow \quad R_f = 1 - 0.64 = 0.36\ \Omega$$

2.8 Diode Resistances

2.8.1 Static Resistance of Diode

Static resistance of diode is defined as ratio of V to I of voltage and current of the diode at operating point. Static resistance of diode at any operating point is equal to the reciprocal of slope of line joining operating point with origin of VI characteristic

$$R_{static} = \frac{V_Q}{I_Q} \tag{70}$$

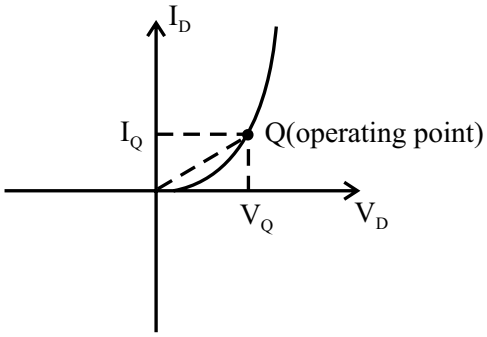


Fig.14 Piecewise linear characteristics of a diode

Note : *Static resistance of a diode is not a useful parameter because it is not constant but depends upon operating point.*

2.8.2 Dynamic Resistance of Diode

Dynamic resistance is also called **incremental resistance** of a diode. It is an important parameter for small signal analysis of the diode. It is applicable for small signal variations around operating point of the diode. The dynamic resistance is reciprocal of slope of V–I characteristic at operating point. Therefore, the dynamic resistance is not constant but depends upon the operating point.

Mathematically, dynamic resistance is given by,

$$r = \frac{d V_D}{d I_D} \tag{71}$$

The diode current under forward biased mode of the diode is given by,

$$I_D = I_o\left(e^{\frac{V_D}{\eta V_T}} - 1\right)$$

Dynamic conductance of the diode can be given as,

$$\therefore \quad g = \frac{d I_D}{d V_D} = I_o \, e^{\frac{V_D}{\eta V_T}} \cdot \frac{1}{\eta V_T} \tag{72}$$

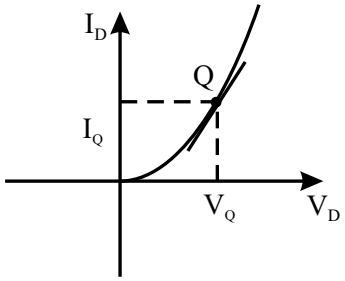


Fig.15 Dynamic characteristics of a diode

$$g = \frac{I_o e^{\frac{V_D}{\eta V_T}}}{\eta V_T} \tag{73}$$

But, $$I_o \, e^{\frac{V_D}{\eta V_T}} = I_D + I_o$$

$$\Rightarrow \quad g = \frac{I_D + I_o}{\eta V_T} \tag{74}$$

The magnitude of reverse saturation current is negligible as compared to forward biased current of the diode.

$$\therefore \quad I_D + I_o \approx I_D$$

$$\Rightarrow \quad \boxed{g = \frac{I_D}{\eta V_T}} \tag{75}$$

The dynamic resistance of the diode is reciprocal of the dynamic conductance. Therefore, the dynamic resistance of the diode,

$$\boxed{r = \frac{1}{g} = \frac{\eta V_T}{I_D}} \tag{76}$$

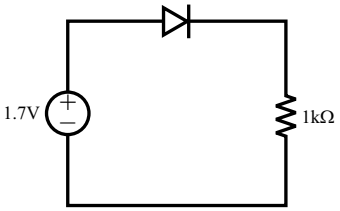
At room temperature, $V_T = 26$ mV

For Ge, $$r = \frac{26}{I_D} \Omega \quad ; \quad \text{where } I_D \text{ is in mA} \tag{77}$$

Note : Take $\eta = 1$ unless it is specified.

Example 12

In the circuit shown below, the ideality factor η of the diode is unity and the voltage drop across it is 0.7 V. The dynamic resistance of the diode at room temperature is approximately

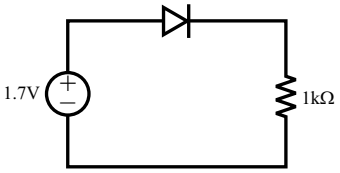


(a) 15 Ω (b) 25 Ω

(c) 50 Ω (d) 700 Ω

GATE(IN/2008/1M)

Solution : Ans.(b)



Diode current in above circuit,

$$I_D = (1.7-0.7) / 1000 = 1 \text{ mA}$$

The dynamic resistance of diode at room temperature of 300 K is given by,

$$r = \frac{\eta V_T}{I_D}$$

where, I_D = forward biased diode current in mA

V_T = Thermal voltage

η = ideality factor = 1 for Ge

At room temperature,

$$V_T = 26 \text{ mV}$$

$$\therefore \quad r = \frac{26}{1} = 26\Omega$$

2.9 Diode Capacitances

2.9.1 Space Charge or Transition Capacitance

The space charge or transition capacitance of a diode is also called barrier or depletion region capacitance. The space charge capacitance plays an important role under reverse biased condition. When a pn junction is reverse biased the majority carriers in p and n layers are moved away from the junction, thereby uncovering more immobile charges of impurity atoms. This uncovering of immobile charges results in increase in depletion layer width may be considered as capacitive effect. Therefore, the transition capacitance arises due to large depletion region around the junction of diode.

Mathematically, transition capacitance is given by,

$$C_T = \frac{\varepsilon A}{W} \tag{78}$$

Where, W is total width of space charge region, A is area of cross section of junction and ε is permitivity of semiconductor material of the diode.

$$\Rightarrow \quad C_T \propto \frac{1}{W} \tag{79}$$

The transition region has the variable width. The width of transition region varies as a function of biasing voltage of diode. Therefore, the transition capacitance is function of biasing voltage.

Case-I : For step graded or abrupt pn junction
The width of depletion layer of an abrupt pn junction is given by,

$$W = \sqrt{\frac{2\in}{q}\left[\frac{1}{N_A}+\frac{1}{N_D}\right]V_j}$$

$$\Rightarrow \quad W \propto V_j^{\frac{1}{2}} \tag{80}$$

where, $V_j = V_o$; for open circuited junction
$V_j = V_o + V_R$; for reverse biased junction
$V_j = V_o - V_F$; for forward biased junction

Transition capacitance, $C_T \propto V_j^{-\frac{1}{2}}$ (81)

Case-II : For linearly graded junction

$$W \propto V_j^{\frac{1}{3}} \tag{82}$$

Transition capacitance, $C_T \propto V_j^{-\frac{1}{3}}$ (83)

2.9.2 Charge Control Description of Diode

Under the forward biased condition, large number of holes are injected from *p*-side to *n*-side. This is called minority carrier injection. For simplicity it is assumed that the concentration of holes on *p*-side is very large as compare to concentration of electrons on *n*-side. Under such assumption most of the current in the junction is due to holes only. So, diode current mostly due to holes current at the junction. The excess holes concentration injected from p-side to n-side reduces exponentially in n-region. The excess minority carrier under this assumption lies only on n-side and is shown as shaded area in region in Fig. 16.

The differential charge due to excess minority charge carriers stored in differential volume Adx can be give by,

$$dQ = \delta p_n(x)Adx \tag{84}$$

Where $\delta p_n(x)$ is excess hole concentration on n-side above its thermal equilibrium value.

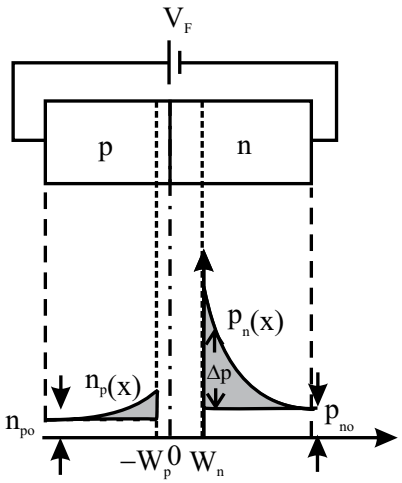


Fig.16 Minority carrier distribution under forward bias.

The excess hole concentration above thermal equilibrium value is given by,

$$\delta p_n(x) = \delta p_n(W_n) e^{-(x-W_n)/L_P} \tag{85}$$

Where, L_p is diffusion length of holes on n-side.

Then the excess charge stored in shaded portion on n-side can be given by,

$$Q = \int_{W_n}^{\infty} Aq\delta p_n(W_n) e^{-(x-W_n)/L_P} dx \tag{86}$$

$$\Rightarrow \quad Q = AqL_p\delta p_n(W_n) \tag{87}$$

The total diode current is sum of diffusion currents of holes and electrons at the junction. If p-side is heavily doped as compared to n-side then total diode current is equal to the hole current at the junction.

$$I = I_{pn}(W_n) + I_{np}(-W_p) \approx I_{pn}(W_n) \tag{88}$$

From equation (53) it is seen that the hole current at junction at $x = W_n$ is given by,

$$I_{pn}(W_n) = \frac{AqD_p(p(W_n) - p_{no})}{L_p} = \frac{AqD_p\delta p(W_n)}{L_p} \tag{89}$$

$$\Rightarrow \quad I_{pn} = \frac{AqL_p\delta p(W_n)}{L_p^{\,2}/D_p} = \frac{AqL_p\delta p(W_n)}{\tau_p} = \frac{Q}{\tau_p} \tag{90}$$

Where, τ_p is mean life time of holes and D_p is diffusion constant of holes.

So, the total diode current,

$$\boxed{I = \frac{Q}{\tau_p}} \tag{91}$$

Thus, the total diode current under forward biased condition is directly proportional to the charge stored due to the excess minority carriers. Therefore, at steady state diode current supplies minority

carriers at the rate at which these carriers are disappearing because of the process of recombination.

Note : *i. The excess minority carriers stored near junction area give rise to a capacitance called diffusion capacitance.*

ii. The injected minority carriers constitute a stored charge Q near the junction area but their is large rate of recombination of minority carrier in the region away from junction on n-side. The rate of recombination of these carriers on n-side controls the forward biasing current of diode under steady state.

iii. When pn junction diode is forward biased the concentration of holes on n-side is higher than than the thermal equilibrium value. So, the charge stored is positive near the junction.

iv. When pn junction diode is reverse biased the concentration of holes reduces to zero near the junction. Thus on p-side of the junction the concentration of holes is less than the thermal equilibrium value and the charge stored is negative near the junction.

2.9.3 Diffusion Capacitance or Storage Capacitance

The diffusion capacitance appears due to storage of excess minority carriers near the junction area outside the depletion layer under forward biased condition. It is also known as **storage capacitance.** The diffusion capacitance of diode plays an important role under forward biased condition.

Mathematically, the diffusion capacitance is given by,

$$C_D = \frac{dQ}{dV} \tag{92}$$

Charge of excess minority carriers stored near junction outside the depletion layer is given by,

$$Q = I\tau \tag{93}$$

Where, I is forward biased diode current.

$$\Rightarrow \quad C_D = \frac{d(I\tau)}{dV} = \tau\frac{dI}{dV} = \tau g = \frac{\tau}{r} \tag{94}$$

Where g is incremental or dynamic conductance, r is incremental or dynamic resistance of the diode and τ is mean life time of holes.

The dynamic resistance of the diode,

$$r = \frac{I_D}{\eta V_T} \tag{95}$$

$$\Rightarrow \quad \boxed{C_D = \frac{\tau}{\eta V_T} I_D} \tag{96}$$

Where, I_D is diode current under forward bias.

$$\Rightarrow \quad C_D \propto I_D \tag{97}$$

Note : So, the diffusion capacitance is proportional to the forward bias current of the diode. As the forward biased current of diode increases more holes will be injected form p-side to n-side and there is more stored charge of excess carriers in n-layer near junction and hence more will be the diffusion capacitance.

Note : Above expression of diffusion capacitance has been derived by assuming stored charge of excess holes on n-side. Similarly, capacitance due to stored charge of excess electrons on p-side can be obtained. In such case total diffusion capacitance will be sum of capacitances due to excess electrons on p-side and excess holes on p-side.

Dynamic diffusion capacitance:

The diffusion capacitance under a dynamic condition is always less than the diffusion capacitance for static signals.

The dynamic diffusion capacitance for a sinusoidal signal at low frequency is given by,

$$\boxed{C'_D = \frac{1}{2}\tau g} \quad (98)$$

For high frequency sinusoidal signals,

$$C'_D = \left(\frac{\tau}{2\omega}\right)^{\frac{1}{2}} g \quad (99)$$

$$\boxed{C'_D \propto \frac{1}{\sqrt{\omega}}} \quad (100)$$

Note:- *(i) Under the forward biased condition $C_D >> C_T$*
So, only diffusion capacitance is taken into account under forward biased condition.
(ii) Under reversed biased mode $C_T >> C_D$
So, only transition capacitance is taken into account under reversed biased condition.

Example 13

Consider an abrupt p-n junction. Let V_{bi} be the built-in potential of this junction and V_R be the applied reverse bias. If the junction capacitance (C_j) is 1 pF for $V_{bi} + V_R = 1V$, then for $V_{bi} + V_R = 4V$, C_j will be

(a) 4 pF (b) 2 pF

(c) 0.25 pF (d) 0.5 pF

GATE(EC/2004/2M)

Solution : Ans.(d)

The depletion layer capacitance of a junction diode is given,

$$C_j = C_T = \frac{\varepsilon A}{W} \quad .....(i)$$

where, ε = permitivity

A = area of cross-section of junction

W = width of the depletion layer

The width of depletion layer,

$$W \propto V_j^{+m}$$

$$\Rightarrow \quad C_j \propto V_j^{-m}$$

where, $m = 1/2$ for step graded or abrupt junction

$= 1/3$ for linearly graded junction

$V_j = V_0$; For no biasing voltage

$= V_0 - V_F$; For forward biased

$= V_0 + V_R$; For reverse biased

V_0 = Barrier potential or built in potential

V_R = reverse biasing voltage

V_F = forward biasing voltage

Therefore, for abrupt junction,

$$C_j \propto (V_0 + V_R)^{-1/2}$$

$$\Rightarrow \quad \frac{C_{j2}}{C_{j1}} = \frac{(V_0 + V_{R2})^{-1/2}}{(V_0 + V_{R1})^{-1/2}}$$

$$\Rightarrow \quad C_{j2} = \frac{(V_0 + V_{R2})^{-1/2}}{(V_0 + V_{R1})^{-1/2}} \times C_{j1} = \frac{(4)^{-1/2}}{(1)^{-1/2}} \times 1 = 0.5\,\text{pF}$$

Example 14

A silicon PN junction diode under reverse bias has depletion region of width 10 μm. The relative permittivity of Silicon, ε_r = 11.7 and the permittivity of free space $\varepsilon_o = 8.85 \times 10^{-12}\ F/m$. The depletion capacitance of the diode per square meter is

(a) 100 μF (b) 10 μF

(c) 1 μF (d) 20 μF

GATE(EC/2005/2M)

Solution : Ans.(b)

The depletion layer capacitance of a junction diode is given,

$$C_T = \frac{\varepsilon A}{W}$$

where, ε = permitivity

A = area of cross-section of junction

W = width of the depletion layer

$$\Rightarrow \quad \frac{C_T}{A} = \frac{\varepsilon}{W} = \frac{8.85 \times 10^{-12} \times 11.7}{10 \times 10^{-6}} = 10\,\mu\text{F/m}^2$$

10. Switching Characteristics of pn Junction Diode

Consider a diode is connected to a voltage source V_{in} through a resistance R_L as shown in Fig. 17. Let initially the input voltage is positive at level V_F. The current through the load is V_F/R_L. Under the forward biased mode excess holes (Δp_n) are stored near junction on n-side of the diode. Let input voltage V_{in} is changed from V_F to $-V_R$ at $t = t_1$. When the supply voltage is reversed the current through the diode immediately starts flowing in reverse direction due to excess minority carriers stored near the junction.

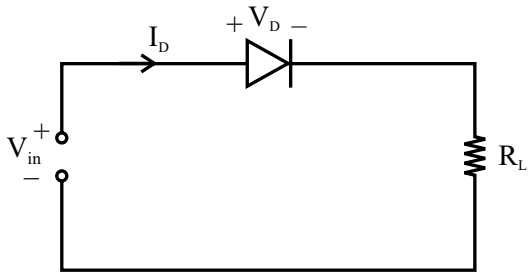


Fig.17 Voltage source feeding load resistance RL through diode

During the period from t_1 to t_2 the excess minority stored in region near the junction are removed. During this period the voltage drop across the diode is positive and very small. This period is known as storage time, t_s. The maximum current in diode during storage time is limited by load resistance R_L and is equal to $-V_R/R_L$. It is time required for discharging of storage capacitance. After removal of excess minority carriers from p and n regions near the junction, the width of transition layer expands during the period from t_2 to t_3 known as transition period, t_r. Transition capacitance is charged during the transition period and voltage across the diode builds up to $-V_R$ and current through the diode reduces to reverse saturation current. Total period from time t_1 to t_3 is called reverse recovery time (t_{rr}) of the diode.

The reverse recovery time of a diode is equal to sum of storage time and transition time. The reverse recovery time of diode plays very important role in switching applications of diode. If the switching time of diode is less than reverse recovery time than diode is never turned off. Therefore, for switching applications the switching time must be more than reverse recovery time of the diode. The reverse recovery time of the diode also restricts its application low frequencies. It should observed from the waveforms of Fig. 18 that maximum power dissipation occurs in the diode during storage time. Since power loss is maximum during turning off process so the losses in the diode are more in switching applications than continuous conduction applications.

The maximum diode current during storage time ,

$$I_{RM} = \frac{-V_R}{R_L} \tag{101}$$

Softness factor of diode:

Softness factor of diode is defined as ratio of transition time to storage time of the diode.

$$S = \frac{t_t}{t_s} \tag{102}$$

Diode with S < 1, *i.e.* $t_t < t_s$ is called fast recovery diode a diode with S = 1, *i.e.,* $t_t = t_s$ is called soft recovery diode.

Total charge stored during reverse recovery time is given by,

$$Q_R = \frac{1}{2} I_{RM}\, t_{rr} \tag{103}$$

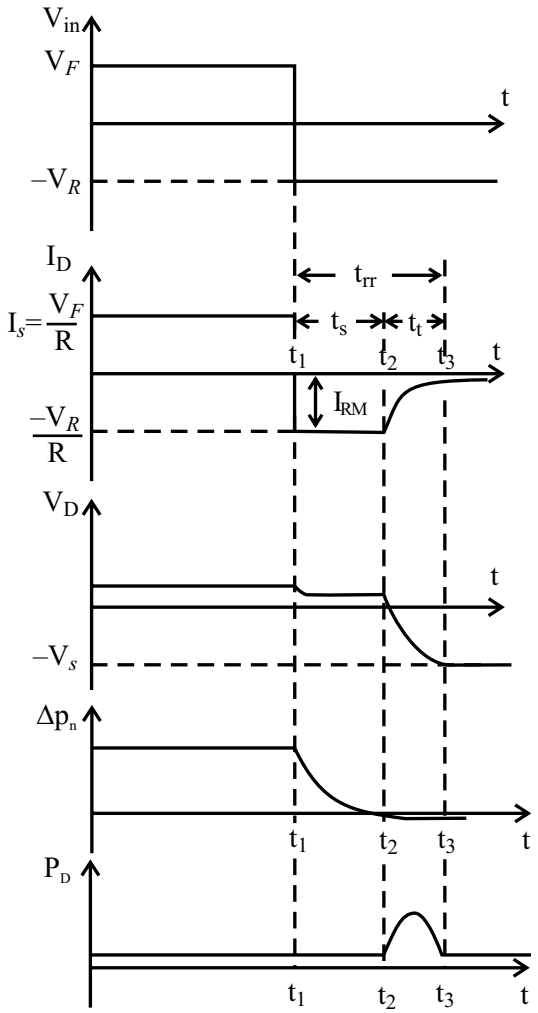


Fig.18 Waveforms of diode voltage, diode current

Where, I_{RM} is the peak reverse current. I_{RM} is related to t_{rr} as under,

$$I_{RM} = t_{rr}.\frac{di}{dt} \tag{104}$$

$$\Rightarrow \quad Q_R = \frac{1}{2} t_{rr}^2 \frac{di}{dt} \tag{105}$$

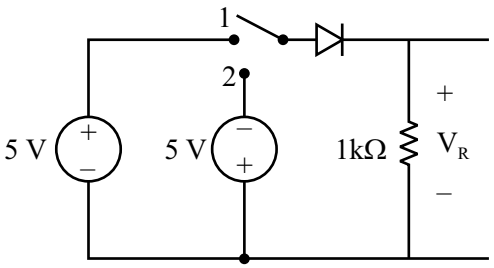
$$\Rightarrow \quad t_{rr} = \sqrt{\frac{2Q_R}{\frac{di}{dt}}} \tag{106}$$

Note : *i. At the time of application of reverse biasing voltage across the diode, the diode current in reverse direction, due to excess minority carriers, is controlled by external load resistance.*

ii. Maximum power dissipation in diode occurs during transition period.

Example 15

In the circuit shown below, the switch was connected to position 1 at $t < 0$ and at $t = 0$, it is changed to position 2. Assume that the diode has zero voltage drop and a storage time t_s. For $0 < t \leq t_s$, V_R is given by (all in Volts)

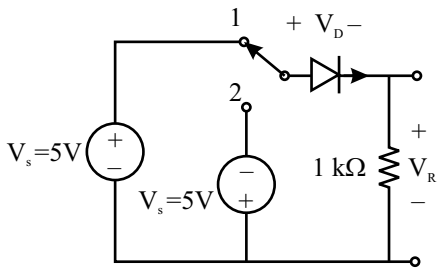


(a) $V_R = -5$ (b) $V_R = +5$

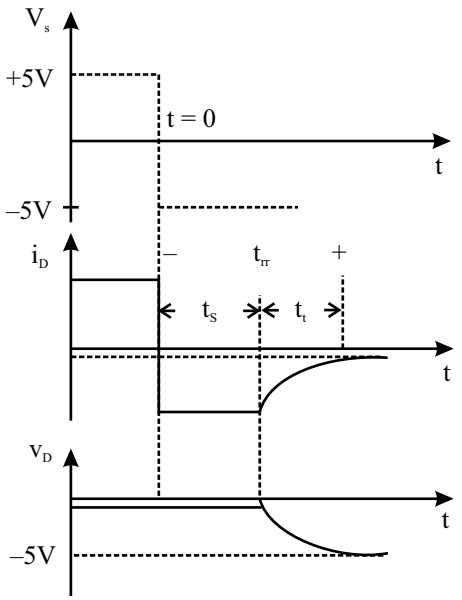
(c) $0 \leq V_R < 5$ (d) $-5 < V_R < 0$

GATE(EC/2006/2M)

Solution : Ans.(a)



Switching characteristic of diode,



Where,

t_{rr} → Reverse recovery time

t_s → Storage time

t_t → Transition time

When diode is reverse biased by changing the position of switch from 1 to 2 at t = 0 the current immediately starts flowing in reverse direction due to excess minority carriers stored in N-layer and diode behaves as short circuit. The current in reverse direction flows until all the excess minority carriers are removed from N-layer. This period is called storage time. Thus, during storage time diode behave as short circuit and, $V_R = -5$ V.

2.11 DC Equivalent Circuit of an Diode

I. Ideal Diode :

An ideal diode behaves as short circuit when it is forward biased and open circuit when it is reverse biased.

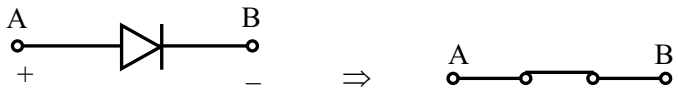


Fig.19 Equivalent circuit if forward biased ideal diode

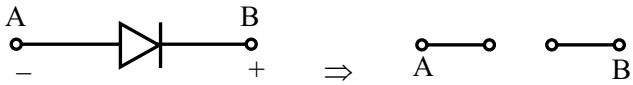


Fig.20 Equivalent circuit if forward biased ideal diode

The VI Characteristics of an ideal diode are as shown below,

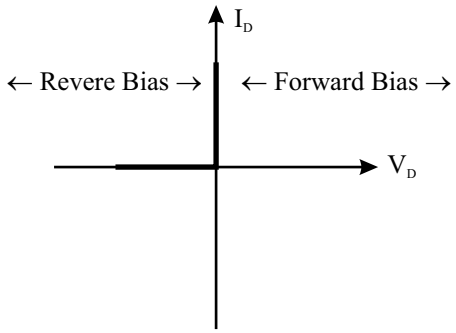


Fig.21 VI characteristics of ideal diode

II. Piecewise Linear Model :

The piecewise linear model represents a battery, a resistance and an ideal diode as shown below,

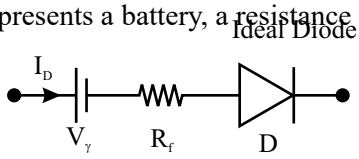


Fig.22 Equivalent circuit of piece wise linear mode of diode

Here V_γ is threshold voltage, R_f is forward resistance of diode and D is ideal diode.

The VI characteristics of piecewise linear model is as shown below,

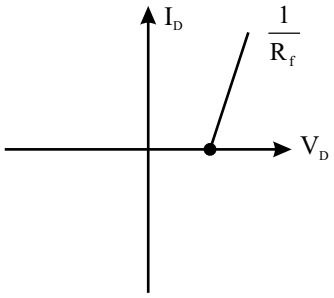


Fig.23 VI characteristics of piecewise linear model of a diode

III. Simplified Model

The diode in a simplified model is represented by a battery of value equal to threshold voltage connected in series with an ideal diodes as shown below,

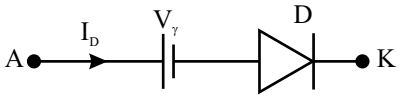


Fig.24 Simplified model of a diode

Here V_γ is threshold voltage and D is ideal diode.

The VI characteristics of simplified model is as shown below,

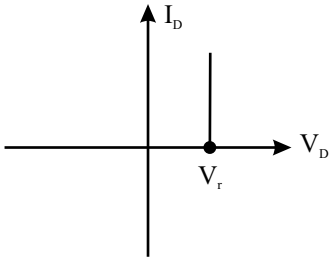


Fig.25 VI characteristics of piecewise linear model of a diode

2.12. Concept of Load Line of Diode

Consider a diode is connected to a DC source through a resistance R_L as shown in the Fig. 26.

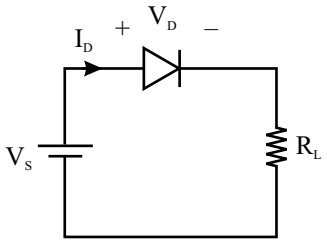


Fig.26 Diode with DC source feeding load R_L.

The current through the diode can be given by,

$$I_D = \frac{V_S - V_D}{R_L}$$

$$\Rightarrow \quad I_D = -\frac{V_D}{R_L} + \frac{V_S}{R_L} \qquad (107)$$

Above equation is called load line of the circuit. It represents a straight line with slope of $-\frac{1}{R_L}$ and intercept at $\frac{V_S}{R_L}$ on I_D axis on the VI characteristics of the diode.

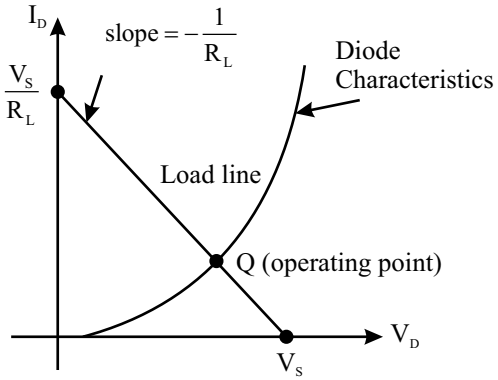


Fig.27 Load line and operating point of diode circuit feeding load R_L

The intersection of load line with VI characteristic curve of the diode is called operating point or Q-point of the circuit as shown in Fig.27.

2.13 Small Signal Model of Diode

The small signal model of a diode is applicable when a diode forward biased with suitable DC source is also subjected to an ac input signal of small amplitude and frequency. Consider a diode is subjected to DC signal V_D and ac signal v_d as shown below. Let v_D is total voltage across the diode and i_D is current through the diode.

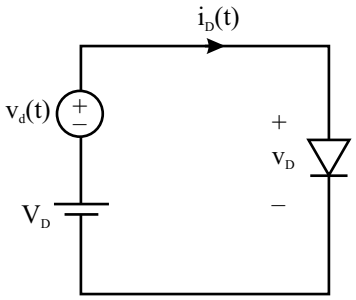


Fig.28 Diode subjected to DC and small signal ac

In absence of ac signal $v_d(t)$, the dc current of the diode,

$$I_D \approx I_0 e^{\frac{V_D}{nV_T}} \tag{108}$$

When $v_d(t)$ is also applied.

$$v_D = v_d + V_o \tag{109}$$

And $$i_D(t) = I_0 e^{\frac{V_D}{nV_T}} = I_0 e^{\frac{v_d + V_D}{\eta V_T}}$$

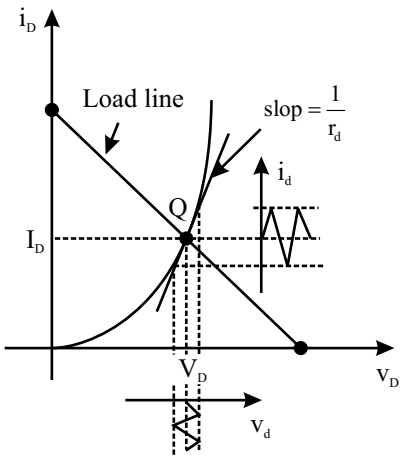


Fig.29 Load line and operating point of diode

$$\Rightarrow \quad i_D(t) = I_0 e^{\frac{V_D}{\eta V_T}} \cdot e^{\frac{v_d}{\eta V_T}} = I_D e^{\frac{v_d}{\eta V_T}} \tag{110}$$

Since v_d is small so, $v_d << \eta V_T$

So $$e^{\frac{v_d}{\eta V_T}} \approx 1 + \frac{v_d}{\eta V_T} \tag{111}$$

$$\Rightarrow \quad i_D(t) = I_D + \frac{I_D}{\eta V_T} \cdot v_d \tag{112}$$

$$\Rightarrow \quad i_D(t) = I_D + i_d \tag{113}$$

Where, $$i_d = \frac{I_D}{\eta V_T} \cdot v_d \tag{114}$$

Dynamic conductance of didoes,

$$g = \frac{d i_d}{d v_d} = \frac{I_D}{\eta V_T} \tag{115}$$

Dynamic resistance of diode,

$$\boxed{r = \frac{1}{g} = \frac{d v_d}{d i_d} = \frac{\eta V_T}{I_D}} \tag{116}$$

Thus small signal equivalent circuit of a diode is a incremental resistance, r.

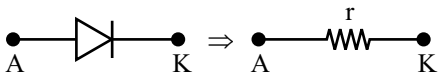


Fig.30 Small signal equivalent resistance of diode

The VI characteristics for small signal model of the diode is as shown below,

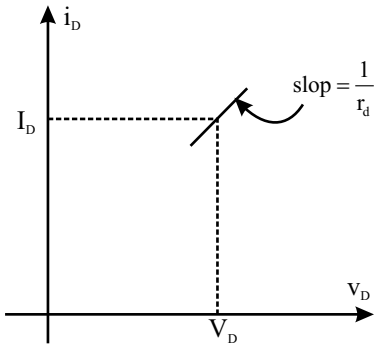


Fig.31 VI characteristics of small signal equivalent circuit of a diode

2.14 Varactor diode

The Varactor diode works on principle of change in transition capacitance due to change in biasing voltage. This diode is also know as Varicap. Since the transition capacitance plays an important role in reverse biasing mode, therefore, varactor diode works in reverse biasing mode in third quadrant of VI characteristic.

The transition capacitance of the diode is related to the junction potential as under,

$$C_T \propto V_j^{\frac{-1}{2}} \text{ ; for step graded junction} \quad (117)$$

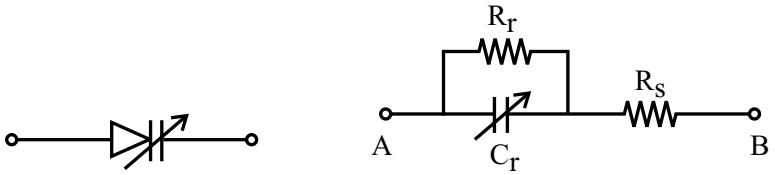
And

$$C_T \propto V_j^{\frac{-1}{3}} \text{ ; for linear junction} \quad (118)$$

Effective junction barrier for reverse biased diode,

$$V_j = V_o + V_R \quad (119)$$

Where V_o is built-in potential of the junction and V_R is reverse biasing voltage of the diode. When the reverse biasing voltage increases the depletion layer width also increases and the transition capacitance reduces.



(a) Symbol (b) Equivalent circuit

Fig.32 Symbol and equivalent circuit of Varactor diode.

Here,

R_R → Resistance of diode in reverse biasing mode

C_r → Junction capacitance i.e., transition capacitance in reverse biasing mode

R_s → Series resistance of body of the diode (metallic mounting's resistance).

Applications :

i. Voltage tuning of LC resonant circuit.

ii. Self balancing bridge circuit.

iii. Voltage control oscillator for generation of FM waves.

iv. Parametric amplifiers for microwave applications.

2.15 Zener Diode

These diodes are also called breakdown diodes. The breakdown diodes are the diodes which are designed to dissipate adequate power to operate in breakdown region under reversed biased mode. These are used as voltage reference or constant voltage devices. Fig. 33 shows the sysmbol of a Zener diode.

Symbol :

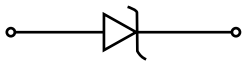


Fig.33 Symbol Zener diode.

2.15.1 V-I characteristic

A Zener diode works under reverse biased mode in third quadrant of vi-characteristic in the breakdown region. The voltage across the diode in breakdown region of operation is equal to the voltage called Zener Voltage, V_z. Thus, the voltage across the diode is fixed at V_z when it is operated in the breakdown region. The current through the diode in breakdown region of operation may vary from I_{zk} to I_{zmax}. The current I_{zk} is knee current of the Zener diode. The VI characteristics of a Zener diode are shown in Fig. 34.

Zener Voltge (V_z) : It is breakdown voltage of the diode.

Knee current (I_{zk}) : The knee current is the minimum current at which the diode is operated in breakdown region. The voltage regulation becomes poor if the diode current falls below the knee current. It is determined by the load voltage.

Maximum current (I_{zmax}) : It is the maximum current through the Zener diode for the safe operation. This current is determined by maximum power dissipation capability of the diode.

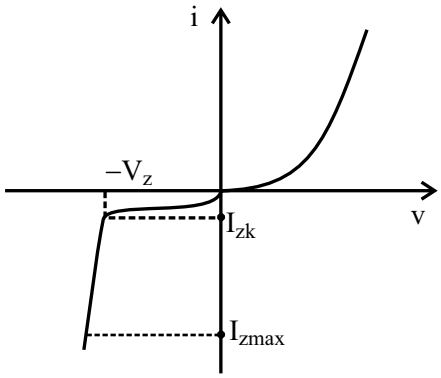


Fig.34 V-I characteristics of Zener diode

2.15.2 Mechanisms of breakdown

Avalanche multiplication: Avalanche multiplication occurs due to collision of thermally generated carriers with lattice atoms. In the process of collision, a new electron-hole pair is generated. The new generated electron-hole pair collides with another lattice atom resulting into breakdown and generating another electron-hole pair. This process becomes cumulative resulting into breakdown of junction called Avalanche multiplication. The Avalanche multiplication occurs in lightly doped semiconductors. The avalanche multiplication generally occurs at voltage greater than 6V. The breakdown voltage of Avalanche multiplication increases with increase in temperature. When the temperature of the diode is increased the thermally generated electron collides with lattice atoms at

the faster rate due to increased lattice vibration. Because of increased rate of collision the electrons are not able to acquire kinetic energy sufficient to knock down the electron from another atom. Therefore, voltage across the diode needs to be increased in order to increase the energy of electron for knocking down another electron. In other words when temperature of the diode is increased, higher voltage is required for avalanche multiplication. Thus the avalanche multiplication has positive temperature coefficient, i.e. breakdown voltage increases with increase in temperature.

Zener Breakdown: This breakdown occurs due to strong applied electric field which results in breaking of covalent bonds of atoms in the depletion region. This breakdown occurs in heavily doped semiconductors diode. When p and n layers of a Zener diode are doped heavily the width of depletion layer is reduced. As electric field in the depletion layer is V/W so the induced electric field in depletion layer is high. Thus a small external voltage of order 6V or less is able to induce an electric field sufficient enough to break the covalent bonds of atoms in the depletion layer resulting in breakdown called Zener breakdown. At high field intensity the force exerted by the field is strong enough to bring out the electrons from the lattice atoms, resulting into generation of electron-hole pairs. Therefore, the Zener breakdown occurs in heavily doped semiconductors at approximate field of 2×10^7 V/m and the voltage less than 6V. When the temperature of Zener diode is increased the energy of electrons is increased and electrons are in excited state due to which a smaller voltage is required to ionize the atoms. Thus, the voltage required for Zener breakdown reduces with increase in temperature. Therefore, Zener breakdown voltage has negative temperature coefficient.

Note : *i. Zener diode works on the principle of tunneling of charge carriers across the junction under the influence of applied reverse biasing voltage which leads to breakdown of the junction.*

ii. The terminology used is always Zener diode for breakdown diodes irrespective of mechanism of breakdown of the diode.

2.15.3 Breakdown Voltage of Zener Diode

Consider a Zener diode with p^+n junction having heavily doped p-side as compared to n-side. It has been observed in previous sections that when p-side is heavily doped then most of the depletion layer lies on n-side. Such type of junction is called one sided junction. The maximum electric field at junction in one sided junction is given by,

$$E_{max} = -\frac{q N_D W_n}{\varepsilon} = -\frac{q N_A W_p}{\varepsilon} \qquad (120)$$

When p-side is heavily doped as compared to n-side the width of depletion layer on n-side of a junction is given by,

$$W_n = \sqrt{\frac{2\varepsilon V_j}{q} \times \frac{1}{N_D}} \qquad (121)$$

Where, $V_j = V_o + V_R$

Putting above expression of W_n in equation (120), we have,

$$E_{max} = -\frac{q N_D}{\varepsilon} \times \sqrt{\frac{2\varepsilon V_j}{q} \times \frac{1}{N_D}} = -\sqrt{\frac{2qN_D V_j}{\varepsilon}}$$

$$V_j = \frac{\varepsilon E_{max}^{\ 2}}{2qN_D}$$

The breakdown of the diode occurs when electric field becomes critical, $E_{max} = E_{cr}$ and reverse bias voltage, $V_j \approx V_R = V_B$

$$\Rightarrow \quad \boxed{V_B = \frac{\varepsilon E_{cr}^{\ 2}}{2qN_D}} \qquad (122)$$

In the above equation V_B represent the reverse breakdown voltage and E_{cr} is critical electric field required for Zener breakdown.

Note : *When n-side is heavily doped and p-side is lightly doped then N_D in above equation is replaced by N_A.*

2.15.4 Dynamic Resistance and Capacitance of Zener diode

Dynamic resistance: It is the resistance offered by the diode in breakdown region. Dynamic resistance of Zener diode is of order of few ohms. Mathematically, it is given by,

$$r_z = \frac{\Delta V_z}{\Delta I_z} \qquad (123)$$

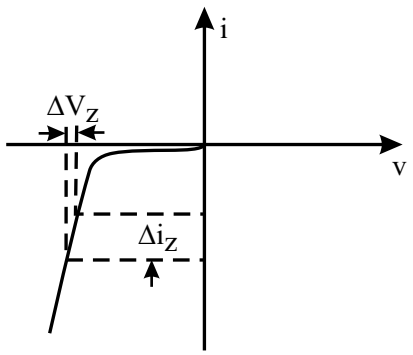


Fig.35 V-I characteristics of Zener diode exhibiting dynamic resistance

Capacitance: As Zener diode works in reverse biased mode therefore the capacitance exhibited by diode is transition capacitance. The transition capacitance of the diode is inversely proportional the depletion layer width and effective potential barrier , V_j at the junction.

$$C_T \propto \frac{1}{W} \qquad (124)$$

and $$W \propto V_j^{\frac{1}{2}} \qquad (125)$$

$$\Rightarrow \quad C_T \propto V_j^{-\frac{1}{2}} \qquad (126)$$

2.15.5 Equivalent Circuit of Zener Diode

A Zener diode working in breakdown region of operation can be represented by dynamic resistance connected in series with a battery of voltage V_Z as shown in Fig. 36.

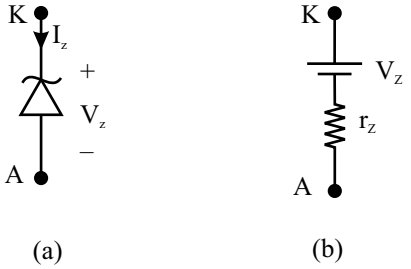


Fig.36 (a) Zener diode (b) Equivalent circuit of zener diode

2.15.6 Applications of Zener Diode

i. Zener diode has a constant voltage drop across it under varying current in breakdown region of operation so when it is connected across a load resistance it acts like a voltage regulator as shown in the Fig 37 below.

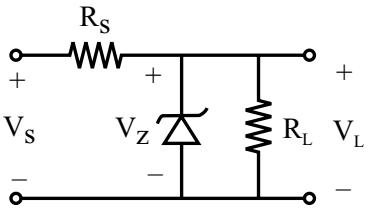


Fig.37 Voltage regulator using Zener diode

ii. Because of constant voltage across the diode in breakdown region it is also used as reference voltage source.

Note : *i. Zener diode is available for voltage greater than 2V. Below 2 V the dynamic resistance of the Zener diode becomes high and voltage regulation becomes poor. For obtaining reference voltage less than 2V, two or more diodes in forward biased mode can be connected in series across the load for voltage regulation.*

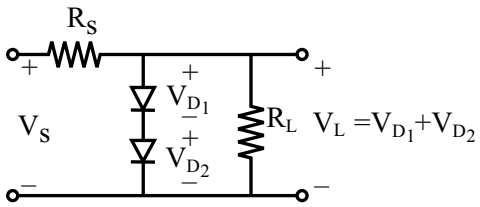


Fig.38 Voltage regulator using forward biased diodes.

ii. For obtaining higher reference voltage beyond voltage rating of a Zener diode, two or more Zener diodes can be connected in series in reversed biased mode.

iii. Series combination of diodes gives higher voltage rating, higher power dissipation, lower temperature coefficient and lower dynamic resistance.

iv. Ideally dynamic resistance of Zener diode is taken to be zero in equivalent circuit unless it is specified.

2.16 Tunnel diode

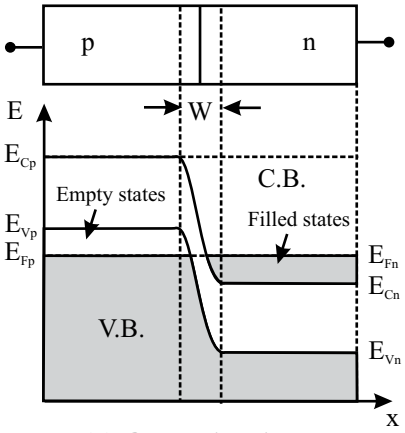
This diode works on the phenomenon of tunneling. In tunnel diode both '*p*' and '*n*' sides are heavily doped as compared to general purpose diode. Because of heavy doping level on both sides of junction. As width of depletion layer is inversely related to doping concentrations the depletion layer width is very small in tunnel diode in comparison to a general purpose diode. Because of narrow width of depletion layer, the probability of penetrating the minority carriers across the junction becomes high and some of the minority carriers jump across the junction to another side. This phenomenon is called tunneling. Diode based on this principle is called tunnel diode.

Note : *A general purpose diode has doping concentrations of order of 1 atom per 10^8 semiconductor atoms whereas the doping concentration is of order of 1 atom per 10^3 semiconductor atoms in tunnel diode.*

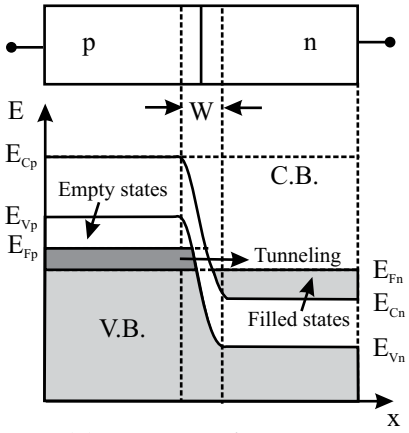
2.16.1 Energy Band Diagram of Tunnel Diode

The doping concentrations of impurity atoms in tunnel diode is kept high so that the Fermi level on p-side lies in the valence band and Fermi level on n-side lies in the conduction band as shown if Fig.39(a) . The operation of tunnel diode can be explained on the basis of shift of Fermi level with biasing of the diode under generate state of the semiconductor. The degenerate state of semiconductor is the state when all the energy states below Fermi level are filled with electrons and all the energy states above the Fermi level are empty.

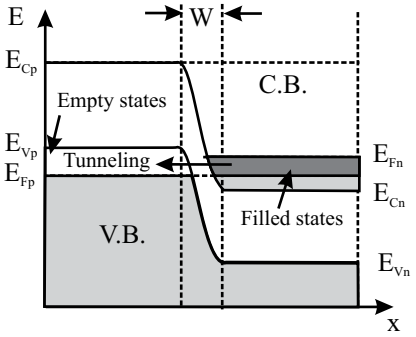
Under open circuited condition Fermi levels on both sides of junction lie at same level as shown in Fig.39(a) and there is no flow of carriers across the junction. When the junction is reverse biased energy levels on n-side shift down ward and energy levels on p-side shift upward as shown in Fig 39(b). So, Fermi level on n-side lies below the Fermi level of p-side. Because of shifting of energy levels there are filled energy states in valence band and empty energy states in conduction band on n-side at same energy level which results in flow of electrons from p-side to n-side. This phenomenon is called tunneling. The change of current is almost linear with reverse biasing voltage in reverse biasing mode of tunnel diode. Therefore tunnel diode behaves like a good conductor in reverse bias mode. When the tunnel diode is forward biased the Fermi level on p-side shifts down ward and Fermi level in n-side shifts upward due to which there are filled energy states in conduction band on n-side and empty energy states in valence band on p-side which results in tunneling of electrons from n-side to p-side as shown in Fig.39(c). The current varies almost linearly up to a forward biasing voltage denoted by V_P in V-I characteristics of the diode shown in Fig.41. The Fermi level shifts upward with increase in forward biasing voltage and forward diode current increases. The current reaches its peak value I_P at voltage V_P where there are maximum number of empty energy states in valence band and filled energy states conduction band as shown in Fig.39(d).



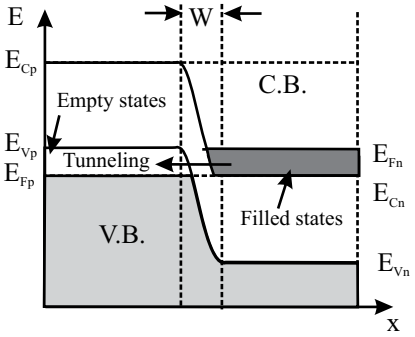
(a) Open circuited



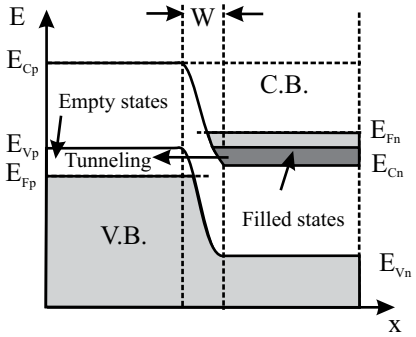
(b) Reverse Biased



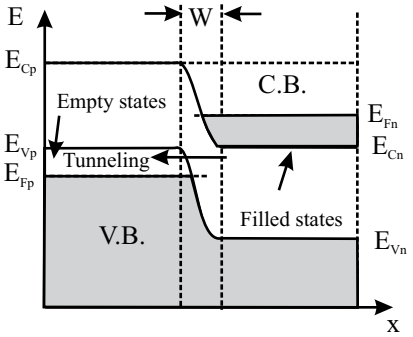
(c) Forward biased with $V < V_P$



(d) Forward biased with $V = V_P$



(e) Forward biased with $V_P < V < V_v$



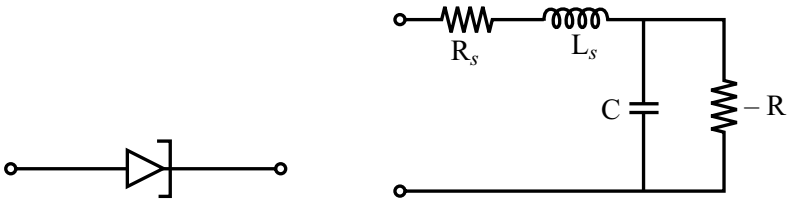
(f) Forward biased with $V = V_v$

Fig.39 Energy band diagrams of tunnel diode under open circuit, reverse biased and forward biased modes

When voltage is increased beyond V_P the current starts decreasing because of shifting of Fermi level further due to which the empty energy states in valence band and filled energy states in conduction band at same energy levels as shown in Fig.39(e) This region of operation of tunnel diode is called negative resistance region of VI characteristics of the diode. When forward biasing voltage is increased further at certain voltage called valley voltage (V_V) the lowest energy level of conduction band on n-side coincide with highest level of valence band on p-side and thus tunneling of carriers

across the junction ceases to exist as shown in Fig.39(f). After the valley voltage the tunnel diode behaves like a normal diode.

2.16.2 Symbol and Equivalent circuit of Tunnel Diode



(a) Symbol (b) Equivalent circuit

Fig. 40 Symbol and Equivalent circuit of tunnel diode.

Where,

R_s is resistance of leads and package of diode.

L_s is inductance of leads and package.

C is capacitance of diode measured at valley point of VI characteristics.

–R is negative resistance of small signal model.

2.16.3 V-I Characteristic of tunnel diode

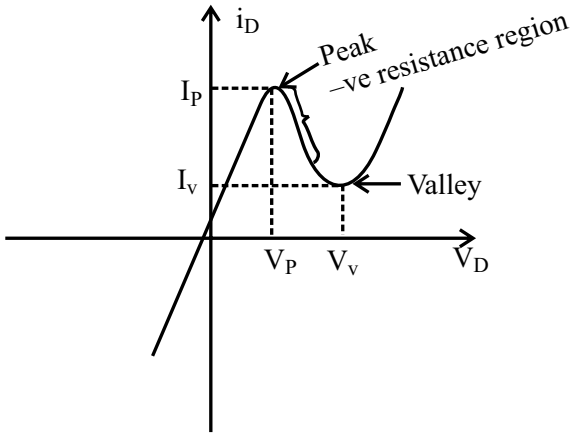


Fig. 41 V-I characteristics of tunnel diode.

i. When forward biasing voltage lies between 0 V and V_p the forward bias current of tunnel diode increases almost linearly from zero to a peak value, I_p.

ii. After peak current the diode exhibit a negative resistance region between voltage V_p and valley voltage V_V where diode current decreases from I_p to I_V with increases in biasing voltage. A tunnel diode is always operated in negative resistance region of VI characteristics under the forward biased mode, in Ist quadrant of VI characteristic.

iii. It behaves like a general purpose diode beyond valley point which is a positive resistance region.

iv. A tunnel diode behaves like a good conductor in reverse biasing mode as VI characteristic is

almost linear in reverse biased mode.

v. The diode characteristic has single value of current for three different values of forward biasing voltage. These characteristic of tunnel diode makes it suitable for pulse and digital circuit.

2.16.4 Applications of Tunnel Diode

i. It can be used as a very high frequency switch with switching time of nanoseconds, therefore, it is used as microwave frequency switch.

ii. It can be used as a microwave frequency oscillator.

Note : *Devices exhibiting negative resistance characteristic can be used as oscillator.*

2.16.5 Advantages and Disadvantages

Advantages:

i. Low cost, low noise, high speed, low power consumption and environmental immunity.

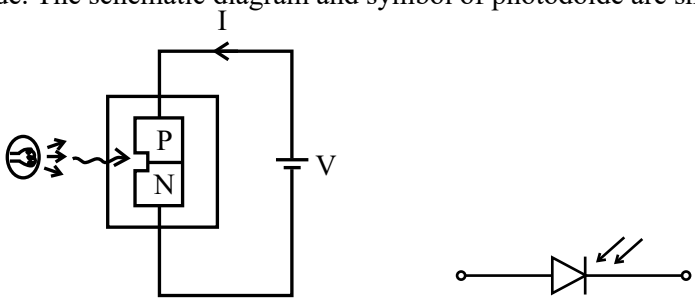
Disadvantages:

i. Low output voltage swing.

ii. Since it is two terminal device, therefore, their is no isolation between input and output.

2.17 PN Junction Photodiode

This diode works on principle of generation of electron-hole pairs due to illumination of the reverse biased pn junction. When junction of a reverse biased pn junction is illuminated with light of suitable wavelength, the number of electron-hole pairs are generated at the junction. These carriers defuse across the junction and form the part of diode current in reverse direction. The diode current increases in reverse direction with increase in intensity of the light. The diode working on this principle is called photodiode. The schematic diagram and symbol of photodoide are shown in figure below.



(a) Schematic diagram (b) Symbol

Fig. 42 Working of photodiode.

Maximum wave length of light required for generation of electron hole pair in photo diode is given by,

$$\lambda_c = \frac{12400}{E_g} \text{ Å} \qquad (127)$$

Where, E_g is band gap in of the semiconductor in electron-volt.

Note : *$1Å = 10^{-10}$ m.*

2.17.1 VI Characteristics of photodiode

A reverse biased diode works in reverse biased mode in third quadrant of VI characteristics. When no source of light is applied in a photodiode only reverse saturation current called dark current flows through the diode. When junction of the photo diode is illuminated, the current in reverse direction increases due to injection of additional generated minority photo electron-hole pairs across the junction. These photo electrons and holes are essentially minority carriers diffusing across the junction. The total current of photodiode is given by,

$$I = -I_{sc} + I_o\left(e^{\frac{V}{\eta V_T}} - 1\right) \quad (128)$$

Where, I_o is reverse saturation current, I_{sc} is short circuited current which due to minority photo generated electron-hole pairs, V is forward biasing voltage. The short circuit current is also known as photo current (I_{photo}). For reverse biased junction, $V = -V_R$ and factor η is 1 for Ge diode and 2 of for Si diode for rated current.

Note : *Short circuit current (I_{sc}) of photo diode is also known as photo-current (I_{photo}) or optical component of current (I_{op})*

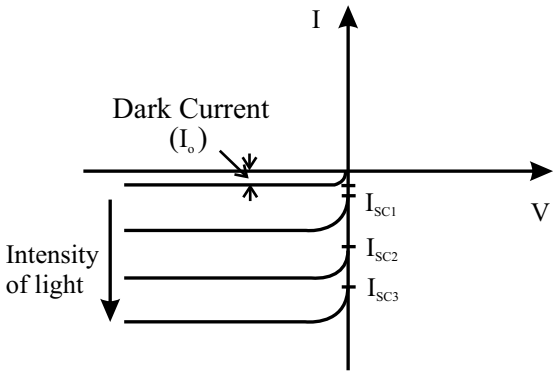


Fig. 43 VI characteristics of photodiode.

Note :
i. Avalanche photodiode works on principle of impact ionization caused by photo electrons.
ii. A photo diode is used in reverse biased mode i.e. the 3rd quadrant of VI characteristic.
iii. The short circuit current of photo diode is proportional to intensity of light.
iv. When diode is not illuminated the component of current which is function of light intensity, (i.e. short circuited current) becomes zero. The remaining component of current in the diode is called dark current. It is approximately equal to reverse saturation current.
v. Variation of current is a function of distance from source of light from the junction.
vi. Photo diode current is function of intensity of light but not of wavelength and frequency. But the wavelength of the light must be less than some critical value, necessary for excitation of the material.

2.17.2 Photo Current and Voltage of Illuminated Photodiode

When a photodiode is uniformly illuminated with light the generation electron-hole pairs result in photo-current of the diode which because of drifting of optically generated electron-hole pairs in depletion layer as well as diffusion of thermally generated minority carriers across the junction which are generated with diffusion length from the junction. If g_{op} is optical generation rate in number charge carriers generated per unit volume per second then number holes generated per second with diffusion length of depletion layer on n-side is AL_pg_{op}. Similarly, the number electrons generated per second with diffusion length of the depletion layer on p-side is AL_ng_{op}. The number of carriers generated with the depletion layer is AWg_{op}. The resulting current due to collection of these carriers at the junction is ,

$$I_{photo} = qAg_{op}(L_p + L_n + W) \tag{129}$$

2.17.3 Performance Parameters of photodiode

I. Responsivity

The responsivity of a photodiode is defined as ratio of photo current (I_{photo})to the power of incident light (P_{op}) at a given wavelength. Mathematically it is given as

$$R_\lambda = \frac{I_{photo}}{P_{op}} \tag{130}$$

The responsivity of photodiode is measure of sensitivity of the diode to light. In other words responsivity is measure of effectiveness of conversion of incident light power to electrical current. It increases slightly with applied reverse bias voltage

II. Quantum Efficiency

Quantum efficiency of a photodiode is defined as fraction of incident photons that contribute to photo-current. It can also be defined as number of carriers collected at the junction for every photon impinging on the photo-detector. Quantum efficiency is an important figure of merit of photo diode.

If J_{photo} is photo-current density then number of carriers arriving at the junction per unit area per second is J_{photo}/q. If P_{in} is incident optical power density in watt per unit area then number of photons impinging on the detector per number area is $P_{in}/h\nu$. Here h is planks constant and ν is frequency of incident light. Then quantum efficiency is is given by,

$$\eta_Q = \frac{J_{photo}/q}{P_{in}/h\nu} \tag{131}$$

If I_{photo} is optical current in A and P_{op} is incident optical power in Watt, then,

$$\eta_Q = \frac{I_{photo}/q}{P_{op}/h\nu} \tag{132}$$

If c is speed of light in semiconductor then the frequency of incident light,

$$\nu = \frac{c}{\lambda} \tag{133}$$

The quantum efficiency can also be obtained using equations (130) & (132) in terms of responsivity

as under,

$$\eta_Q = \frac{R_\lambda}{q} \times h\nu = \frac{R_\lambda}{q} \times \frac{hc}{\lambda}$$

Putting, $h = 6.62 \times 10^{-34}$ joule-seconds, $c = 3 \times 10^8$ m/s and $q = 1.6 \times 10^{-19}$ in above equation, we have,

$$\eta_Q = 1.240 \frac{R_\lambda}{\lambda} \quad (134)$$

Where λ is wavelength of incident light in μm.

2.17.4 Relation in Solar Intensity and Photocurrent

The photo current of a photodiode is directly proportional to the intensity of light falling on the diode.

$$I_{photo} \propto I_v(x) \quad (135)$$

$$\Rightarrow \quad I_{photo} = kI_v(x) \quad (136)$$

Where k is constant of proportionality.

The intensity of light is measure or photon flux is measured in energy/cm^2-s or Watt/cm^2.

The intensity of light is decreases exponentially inside semiconductor. The intensity of light at any distance x from the surface inside the semiconductor is given by,

$$I_v(x) = I_{vo} e^{-\alpha x} \quad (137)$$

Where I_{vo} is intensity at surface and α is the absorption coefficient.

The intensity of a light falling on the surface of the semiconductor also reduces when the distance between light source and surface of semiconductor is increased. Therefore, the diode current reduces as distance of the source is increase from the surface of the semiconductor as shown in the figure below,

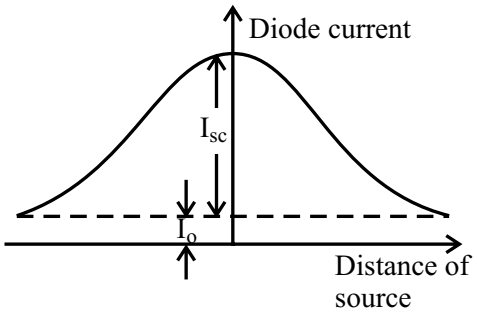


Fig. 44 Photodiode current as function distance from photodiode.

2.17.5 Applications of photodiode

i) Light detection system.
ii) Reading of film sound track
iii) Production line counting of the objects.
iv) High speed reading of computer punch card.
v) Photo voltaic cells or solar cells.

Example 16

When the optical power incident on a photodiode is 10μ W and the responsivity is 0.8 A/W, the photocurrent generated (in μA) is_____

GATE(EC-I/2014/1M)

Solution : Ans.(7.99 to 8.01)

The current of photodiode in terms of optical incident power and responsivity is given by,

$$I_{photo} = (\text{optical incident power}) \times \text{responsivity}$$

Given, optical incident power $= 10\mu$ W

$$\text{responsivity} = 0.8 \text{ A/W}$$

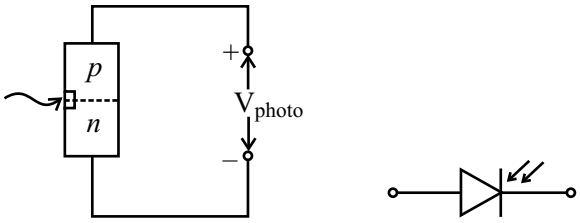
$$\Rightarrow \quad I_{photo} = 10 \times 0.8\ \mu A = 8\ \mu A$$

2.18 Photovoltaic cell or Solar Cell

A photovoltaic cell or solar cell is a semiconductor devices which generates voltage when illuminated with a light. The functioning of a solar cell is similar to a photodiode. It is a photodiode which is unbiased and connected to a load. However, there solar cell is different from photodiode in the sense that it works on a wide spectrum unlike photodiode which works on narrow range of wavelength. It has wide area of expose to light as compared to a photodiode. For a photo diode quantum efficiency is prime where as power conversion efficiency is prime for a solar cell.

2.18.1 Working Principle of Solar Cell

When the junction of an open circuited photodiode is illuminated with light there is generation of electron hole pairs in depletion layer. The photo generated additional electrons drift through depletion layer from p-side to n-side and holes from n-side to p-side under influence of built in potential and results in reduction of potential barrier. The reduction in potential barrier appears across the terminals of diode as induced voltage called photovoltage. This induced potential is called photo voltaic potential and the device working on this principle is called photo voltaic cell or solar cell. The anode becomes positive terminal and cathode becomes negative terminal due to induced photovoltage potential in a photodiode. The schematic diagram and symbol of photovoltaic cell are shown in figure below.



(a) Schematic Diagram **(b) Symbol**

Fig. 45 Photovoltaic or solar cell.

Note : *i. In photo voltaic cell the terminal on p-side of junction is positive and n-side is negative due to induced photovoltaic potential. Therefore, current in the outer circuit flows from p-side to n-side.*

Inside the diode it flows from n-side to p-side.

ii. The barrier potential of diode has p-side negative and n-side positive.

2.18.2 Photovoltaic Potential or Photo voltage

Current through a photo diode from p to n side in the diode is given by,

$$I = -I_{sc} + I_o(e^{\frac{V}{\eta V_T}} - 1) \quad (138)$$

When photodiode is used as photovoltaic or solar cell the terminal of the diode are open circuited and junction is illuminated with light source. Under such conditions the current in diode is zero and voltage induced across the terminals is called photovoltaic potential. Replacing V by V_{photo} and setting I = 0 in equation (138), we have,

$$\Rightarrow \quad -I_{sc} + I_o(e^{\frac{V_{photo}}{\eta V_T}} - 1) = 0$$

$$\Rightarrow \quad I_o e^{\frac{V_{photo}}{\eta V_T}} = I_{sc} + I_o$$

$$\Rightarrow \quad \boxed{V_{photo} = \eta V_T \ln\left(1 + \frac{I_{sc}}{I_o}\right)} \quad (139)$$

Where, I_{sc} is short circuited current or photo current of the cell. Here V_{photo} is open circuited voltage so it is also denoted by V_{oc}.

The photo voltage or open circuited voltage of solar cell can also be written in terms of current density as under,

$$\boxed{V_{photo} = \eta V_T \ln\left(1 + \frac{J_{sc}}{J_o}\right)} \quad (140)$$

Where, J_{sc} is short circuited current density and J_o is reverse current density.

Note : V_{photo} also relates to optical generation rate and thermal generation rate as under,

$$\boxed{V_{photo} = \eta V_T \ln \frac{g_{op}}{g_o}} \quad (141)$$

Where $g_{op} = \delta p/\tau_n$ = optical generation rate and $g_o = p_o/\tau_n$ = thermal generation rate at thermal equilibrium.

2.18.3 V-I Characteristics of Photovoltaic or Solar Cell

The VI characteristics of a solar cell can be obtained by connecting a forward biasing variable voltage source across terminals of the cell as shown in Fig. 46.

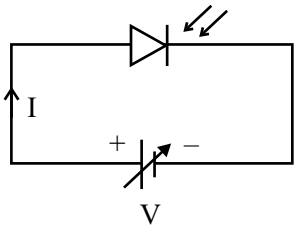


Fig. 46 Circuit for obtaining VI characteristics of solar cell.

When V = 0 , the current through the cell is maximum called short circuited or photo current. When biasing voltage V is increased the current in the circuit starts decreasing. When voltage across the terminals becomes equal to V_{photo} or V_{OC} the diode current becomes equal to zero. V_{photo} is maximum or open circuited voltage induced across the solar cell. The V-I characteristics of the solar cell are as shown in Fig.47.

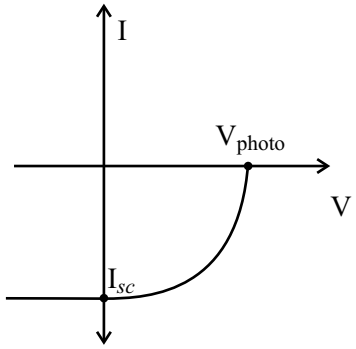


Fig. 47 V-I characteristics of solar cell.

Note :
i. Photo voltaic cell or solar cell works in fourth quadrant of V-I characteristic.
ii. A solar cell behaves like constant current source in 3rd quadrant of VI characteristic i.e. under reverse biased mode.
iii. The photo voltaic potential for Si is 0.5 V and for Ge is 0.1 V.
iv. For getting the higher voltages multiple cells are connected series.
v. For getting current rating higher than short circuited current I_s of a cell, multiple photo voltatic cells are connected in parallel.
vi. Devices are connected in series to increase voltage rating and connected in parallel to increase current rating.
vii. Photo voltaic cell is the only cell which can work even under short circuited condition.
viii. Photo voltaic cell is called solar cell. The photo voltaic cell converts light energy to electrical energy.

2.18.4 Output Power, Conversion Efficiency and Fill Factor of Solar cell

When a solar cell is directly connected across a load resistance R_L then the output power of solar cell can be given by,

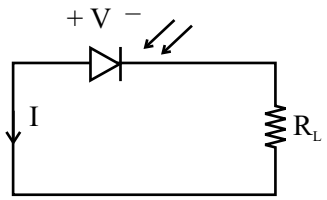


Fig. 48 Solar cell connected to a load,R_L.

$$P = VI = V\left(I_{sc} + I_o(1 - e^{\frac{V}{\eta V_T}}) \right) \quad (142)$$

Where V is voltage induced in the cell and I is current supplied by the cell.

$$P = I^2R_L = \frac{V^2}{R_L} \quad (143)$$

When a solar cell is directly connected across a load resistance R_L the output power is zero when R_L is replaced either by a short circuit or by an open circuit. The power supplied by the cell is maximum (P_m) only at some optimum value of R_L. Let the voltage and current corresponding to maximum power are V_m and I_m respectively.

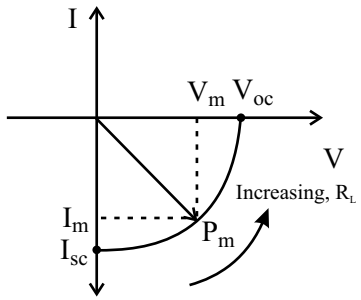


Fig. 49 Maximum power rectangle of solar cell

Fill Factor :

Fill factor of solar cell is defined as maximum output power of cell to the product $V_{oc}I_{sc}$.

$$\therefore \quad \text{Fill factor} = \frac{P_{max}}{V_{OC}I_{SC}} = \frac{V_mI_m}{V_{OC}I_{SC}} \quad (144)$$

Conversion Efficiency:

The conversion efficiency of a solar cell is defined as ratio of output power of the cell to the input solar power to the cell. The efficiency is maximum when the output power is maximum.

$$\eta_c = \frac{P_{out}}{P_{in}} \times 100 \quad (145)$$

Maximum efficiency of solar cell,

$$\eta_{c,max} = \frac{V_mI_m}{P_{in}} \times 100 \quad (146)$$

Example 17

In full sunlight, a solar cell has a short circuit current of 75 mA and a current of 70 mA for a terminal voltage of 0.6 V with a given load. The Thevenin's resistance of the solar cell is

(a) 8 Ω (b) 8.6 Ω

(c) 120 Ω (d) 240 Ω

GATE(IN/2007/1M)

Solution : Ans.(c)

Let V_{OC} is open circuit voltage of solar cell and R_{TH} is equivalent Thevenin resistance of cell. Then,

$$\frac{V_{OC}}{R_{TH}} = 75 \times 10^{-3}$$

$$\Rightarrow \quad V_{oc} = 75 \times 10^{-3} R_{TH} \quad \text{.....(i)}$$

And $$\frac{V_{OC} - 0.6}{R_{TH}} = 70 \times 10^{-3}$$

$$\Rightarrow \quad Voc - 0.6 = 70 \times 10^{-3} R_{TH} \quad \text{.....(ii)}$$

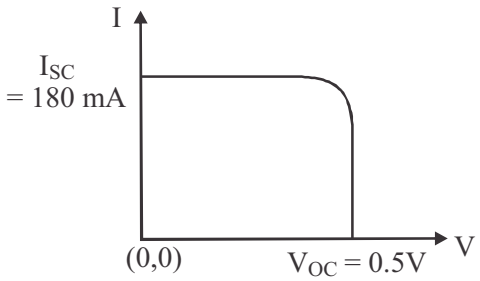
From (i) and (ii) , we have,

$$75 \times 10^{-3} R_{TH} - 0.6 = 70 \times 10^{-3} R_{TH}$$

$$R_{TH} = 120\ \Omega$$

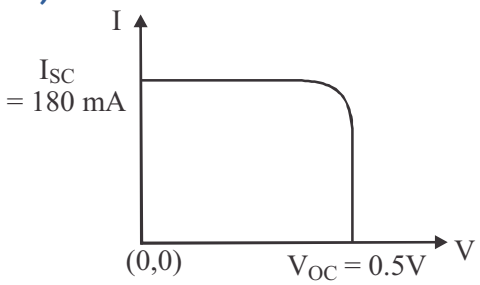
Example 18

The figure shows the I-V characteristics of a solar cell illuminated uniformly with solar light of power 100 mW/cm^2. The solar cell has an area of 3 cm^2 and a fill factor of 0.7. The maximum efficiency (in %) of the device is .....



GATE(EC-III/2016/1M)

Solution : Ans. (20.5 to 21.5)



From I-V characteristic curve,

Open circuited or photo voltage of cell,

$$V_{OC} = 0.5 \text{ V}$$

Short circuited or photo current,

$$I_{SC} = 180 \text{ mA} = 0.18 \text{ A}$$

Input solar power, $P_{in} = 100 \text{ mW/cm}^2$

Area of solar cell, $A = 3 \text{ cm}^2$

Fill factor, $F = 0.7$

Fill factor of a solar cell is given by,

$$F = \frac{P_{max}}{V_{OC} I_{SC}}$$

Where, P_{max} is maximum output power of cell.

$$\Rightarrow \quad P_{max} = FV_{OC}I_{SC} = 0.7 \times 0.5 \times 180 \text{ mW} = 63 \text{ mW}$$

Input power of the given cell,

$$P_{in} = 100 \times 3 = 300 \text{ mW}$$

Maximum efficiency of the device,

$$\eta_{max} = \frac{P_{max}}{P_{in}} \times 100 = \frac{63}{300} \times 100 = 21\%$$

Example 19

For a particular intensity of incident light on a silicon pn junction solar cell, the photocurrent density (J_L) is 2.5 mA/cm^2 and the open-circuit voltage (V_{oc}) is 0.451 V. consider thermal voltage (V_T) to be 25mV. If the intensity of the incident light is increased by 20 times, assuming that the temperature remains unchanged. V_{oc} (in volts) will be _____.

GATE(EC-II/2017/2M)

Solution : Ans. (0.51 to 0.62)

The open circuited or photo voltage of a solar cell is given by,

$$V_{oc} = \eta V_T \ln\left(1 + \frac{I_{sc}}{I_o}\right) = \eta V_T \ln\left(1 + \frac{J_{sc}}{J_o}\right)$$

Given, $V_{oc} = 0.451 \text{ V}, I_{sc} = 2.5 \text{ mA/cm}^2$

$V_T = 25\text{mV}$, As η is not specified so take it 1.

$$\Rightarrow \quad 0.451 = 0 \ 25 \times 10^{-3} \ln\left(1 + \frac{2.5 \times 10^{-3}}{J_o}\right)$$

$$\Rightarrow \quad J_o = 3.65 \times 10^{-12} \text{ A/cm}^2$$

The photocurrent of a solar cell is directly proportional to the intensity of light falling on it. If intensity of light is increased 20 times then the photo current also increases 20 times of its initial

value. If initial photo current density is 2.5 mA/cm^2 then the photocurrent density after increase of intensity by 20 times becomes 20×2.5 mA/cm^2

Then the open circuited voltage becomes as under,

$$V_{oc} = 25\times10^{-3}\ln\left(1+\frac{20\times2.5\times10^{-3}}{3.65\times10^{-12}}\right) = 0.583\ \text{V}$$

Example 20

Quantum efficiency of a photodiode (ratio between the number of liberated electrons and the number of incident photons) is 0.75 at 830 nm. Given Plank's constant h = 6.624 × 10^{-34} J, the charge of an electron e = 1.6 × 10^{-19} C and the velocity of light in the photodiode c_m = 2 × 10^8 m/s. For an incident optical power of 100 μW at 830 nm, the photocurrent in μA is _____.

GATE(IN/2017/2M)

Solution : Ans. (74.5 to 75.5)

The quantum efficiency of a photodiode is given by,

$$\eta_Q = \frac{I_{op}/q}{P_{op}/h\nu}$$

Where I_{op} is photo current, P_{op} is incident optical power, ν is frequency of incident light. which is c/λ

$$\Rightarrow \quad I_{op} = q\eta_Q\frac{P_{op}}{h\nu}$$

Frequency of input light is given by,

$$\nu = \frac{c}{\lambda}$$

Where c is speed of light in semiconductor.

$$\Rightarrow \quad I_{op} = q\eta_Q\frac{P_{op}}{hc}\lambda$$

$$\Rightarrow \quad I_{op} = \frac{1.6\times10^{-19}\times0.75\times100\times10^{-6}\times830\times10^{-9}}{6.624\times10^{-34}\times2\times10^{8}} = 75.18\mu\text{A}$$

2.19 Schottky Diode

The Schottky barrier diode is a metal to semiconductor junction diode. This diode is also called point contact diode. Metal to semiconductor junction can be of 2 types *i.e.* either rectifying type or ohmic contact. In most of the case the rectifying contact are made between metal and n-type semiconductors.

Conditions for metal to semiconductor junction to be rectifying:

Case-I : n-type semiconductors

Junction between a metal and *n*-type semiconductor is rectifying type when work function of metal is more than the work function of semiconductor.

i.e. $\boxed{\phi_m > \phi_s}$ (147)

Where ϕ_m is work function of metal which is energy required to move electron from Fermi level to surface of metal and ϕ_s is work function of semiconductor which is energy required to move electron from Fermi level to surface of the semiconductor.

Note : *Metal to n-type semiconductor contact is ohmic in nature when*

$$\boxed{\phi_m < \phi_s} \tag{148}$$

Case-II : p-type semiconductors

Junction between metal to p-type semiconductor is rectifying in nature when work function of metal is less than the work function of semiconductor.

i.e. $$\boxed{\phi_m < \phi_s} \tag{149}$$

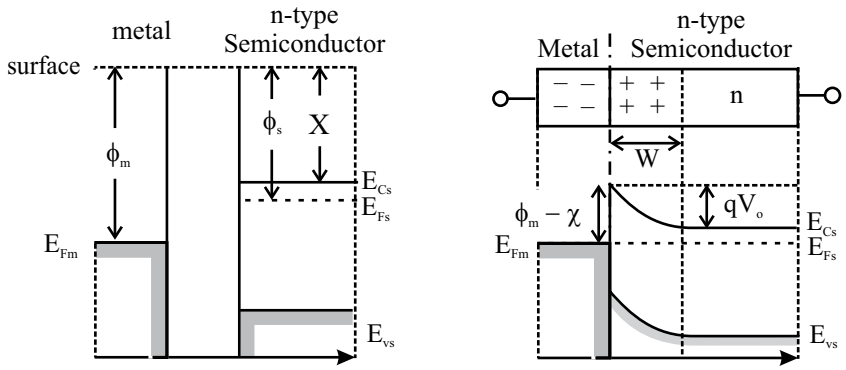
Note : *Metal to p-type semiconductor contact is ohmic when*

$$\boxed{\phi_m > \phi_s} \tag{150}$$

2.19.1 Energy Band Diagram of Open Circuited Schottky Diode

Case-I : Metal to n-type semiconductor rectifying junction

The metal to n-type junction is rectifying when the work function of metal is more than that of the semiconductor, i.e. $\phi_m > \phi_s$. Under such conditions the Fermi level of semiconductor is more than that of the metal as shown in Fig.50(a) When metal and semiconductor are brought in contact with each other the electrons from semiconductor moves to metal side and Fermi level of semiconductor is lowered to align itself with Fermi level of metal as shown in Fig.50(b). During this process a potential barrier is developed across the junction.



(a) Before joining (b) After joining

Fig. 50 Energy band diagram of metal and n-type semiconductor (a) before joining and (b) after joining

The built in potential which prevents further diffusion of electrons form semiconductor to metal is given by,

$$V_o = q\phi_m - q\phi_s \tag{151}$$

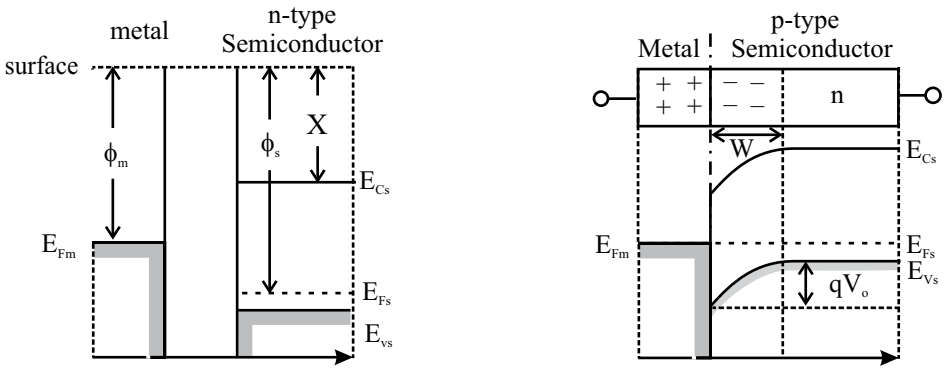
The ideal potential barrier seen by an electron which is trying to jump from metal to semiconductor conduction band is given by,

$$q\phi_{Bo} = q\phi_m - q\chi \tag{152}$$

Where χ is called electron affinity of semiconductor which is energy required to move electron from conduction band to surface of semiconductor.

Case-II : Metal to p-type semiconductor rectifying junction

The metal to p-type junction is rectifying when the work function of metal is less than that of the semiconductor, i.e. $\phi_m < \phi_s$. Under such conditions the Fermi level of semiconductor is less than that of the metal as shown in Fig.51(a). When metal and semiconductor are brought in contact with each other the electrons from metal move to semiconductor side and Fermi level of semiconductor shifted upward to align itself with Fermi level of metal as shown in Fig.51(b).

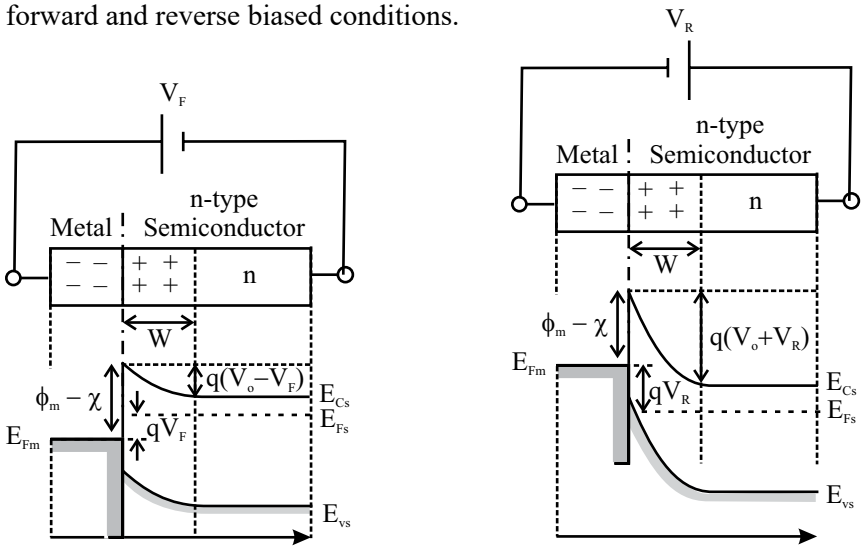


(a) Before joining (b) After joining

Fig. 51 Energy band diagram of metal and p-type semiconductor (a) before joining and (b) after joining

2.19.2 Energy Band Diagram of Forward Biased and Reverse Biased Schottky Diode

The energy band diagram of metal to n-type semiconductor junction Schottky diode is shown in Fig. 52 under forward and reverse biased conditions.



(a) Forward Biased (b) Reverse Biased

Fig. 52 Energy band diagram of Schottky Diode (a) Forward biased (b) Reverse biased

When the junction is forward biased with metal connected to positive terminal of the battery, the Fermi level on semiconductor side is shifted upward. The difference between Fermi levels on metal side and semiconductor side is qV_F. When the junction is reverse biased the Fermi level on semiconductor side shifts down ward and difference between Fermi levels is qV_R.

2.19.3 Working of Schottky Barrier Diode

Most of the Schottky barrier diodes are fabricated with metal on one side and a n-type semiconductor on other side. So, working of metal to n-type semiconductor Schottky barrier diode has been discussed in this section. When metal side is connected to positive terminal and n-type semiconductor is connected to negative terminal the diode behaves like a forward biased pn junction diode. Here the electrons from n-type semiconductor are injected in to the metal resulting into forward biased current. Unlike a pn junction diode current in Schottky diode carriers current due to thermoionic emission of majority carriers in forward biased condition due to which is also called a unipolar device. It is also known as hot carrier device.

Since current is due to majority carriers so it does not have minority carriers storage under forward biased condition so the diffusion or storage capacitance is absent in Schottky diode. Due to absence of diffusion or storage capacitance the storage time is nil hence the reverse recovery time is negligible in case of s Schottky diode. Therefore, the switching speed of Schottky diode is very high as compared to a simple pn junction diode. It is used as a low level detector.

Note:

i. Schottky diode is majority carrier unipolar device.

ii. Current in Schottky diode is due to majority carriers whereas current in pn diode is due to diffusion of minority carriers across the junction.

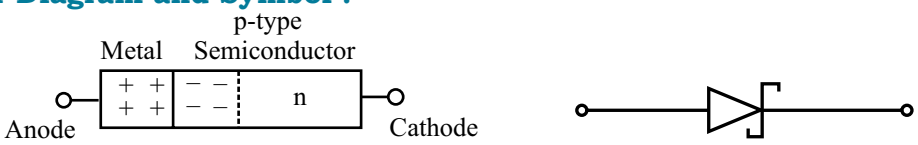
iii. The Schottky diode has larger reverse saturation current as compared to a general purpose pn junction diode.

iv. The cut in voltage of Schottky diode is less than a general purpose pn junction diode.

v. The Schottky diode has no storage capacitance due to which its switching speed is very high as compared to a general purpose diode. So, Schottky diode has better high frequency response than a general purpose diode.

vi. The expression of electric field intensity and depletion layer width of Schottky diode are same as that of a pn junction diode.

Layer Diagram and Symbol :



(a) Layer Diagram **(b) Symbol**

Fig. 53 Layer diagram and symbol of Schottky barrier diode

V-I Characteristics :

The characteristics of Schottky barrier diode are similar to that of pn junction diode however it has larger saturation current and small cut-in voltage than a general purpose diode.

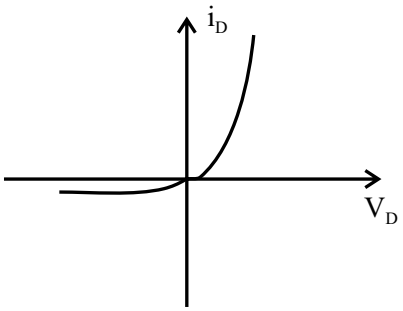


Fig. 54 V-I characteristics of Schottky barrier diode

Forward Bias current :

The forward bias current density of a Schottky barrier diode is given by,

$$\boxed{J = J_{sT}\left(e^{\frac{V}{V_T}} - 1\right)} \quad (153)$$

Where J_{sT} is reverse saturation current density. The reverse saturation current in Schottky barrier increases with increase in reverse biasing voltage due to barrier lowering effect.

Metals used for Schottky diode:

The commonly used metals are Aluminum, Gold and Silver.

Applications :

i. Schottky diode is used in wave shaping circuits.
ii. It is connected between base and collector of BJT to avoid saturation of BJT in digital circuits. Such BJT is called Schottky clamped transistor. A Schottky clamping of transistor with Schottky diode prevent the transistor from full saturation, eliminate saturation delay time and achieve better switching speed.

2.20 Light Emitting Diode (LED)

A light emitting diode works on the principle of emission of light from a forward biased junction due to recombination of electrons and hole pairs. When a diode is forward biased there is minority carrier injection. When minority carriers are injected across the junction there is large recombination of minority carriers with majority carriers near the junction area. A radiation is emitted during this recombination which may lie in visible spectrum. The diode emitting radiation in visible spectrum are used as light emitting diode (LED). The intensity of light emitted by LED is proportional to the forward biased diffusion current of the the diode.

Wavelength of light emitted by LED is given by,

$$\lambda_c = \frac{12400}{E_g}A^\circ = \frac{1.24}{E_g}\mu m$$

Mostly compound of Galium such as GaAsP, GaAlAs etc are used for fabrication of LEDs. GaAs (Gelium Arsenide), GaP (Gelium Phosphide) are most commonly used materials for the fabrication of light emitting diodes. GaAs and InSb, InP emit infrared radiation where as GaP emits visible (i.e.

green) light. GaAs is direct band gap semiconductor and GaP is indirect band gap semiconductor.

Symbol :

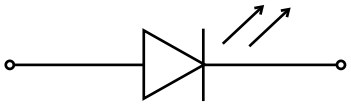


Fig. 55 Symbol of LED

Example 21

The band gap in eV of a semiconductor material required to construct an LED that emits peak power at the wavelength of 620 nm is .....

(Plank constant h = 4.13567×10^{-15} eV s and speed of light c = 2.998×10^{8} m/s)

GATE(IN/2016/2M)

Solution : Ans. (1.9 to 2.1)

The wavelength of light emitted by LED is given by,

$$\lambda = \frac{hc}{E_g}$$

Where, E_g is energy gap in eV

$$\Rightarrow \quad E_g = \frac{hc}{\lambda} = \frac{4.13567\times10^{-15}\times2.998\times10^{8}}{620\times10^{-9}} = 2 \text{ eV}$$

2.21 PIN diode

The PIN diode differs from the basic PN junction diode in the sense that it has a high resistance intrinsic layer I between P and N layers as shown in Fig 56. As a result of the intrinsic layer, PIN diodes have a high breakdown voltage and exhibit a low level of junction capacitance. In addition to this the larger depletion region of the PIN diode is ideal for applications as a photodiode.

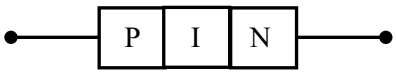


Fig. 56 PIN diode

Here P for p-type semiconductor, I for intrinsic layer and N for n-type semiconductor. The intrinsic layer provides the possibility of high electric field between P and N region. Due to the intrinsic layer electron-hole pair generation is enhanced enabling the diode to process even weak signals. Since the separation between P and N regions is large. Therefore, the capacitance between P and N region, is small. The small capacitance between P and N region allows the diode to operate at very high frequencies. This diode can be used as a microwave frequency switch at frequencies exceeding 300 MHz. When the diode is reverse biased, the thickness of depletion layer is increased until the entire intrinsic region is sweep out and becomes free of mobile charge carriers. The reverse biasing voltage required to sweep out the mobile carriers from the intrinsic region is called sweep out voltage. In

most microwave applications sweeping out of intrinsic region is necessary otherwise a current flows due to mobile carriers in high resistivity intrinsic region resulting in loss of the signal. Because of this characteristic PIN diode is use as microwave switch under reverse biased condition. Intrinsic layer between P and N regions makes it suitable for attenuators, fast switches, photodetectors, and high voltage power electronics applications

❐❐❐

GATE PRACTICE QUESTIONS

Q.1 In a uniformly doped abrupt p-n junction, the doping level of the n-side is four (4) times the doping level of the p-side. The ratio of the depletion layer widths is

(a) 0.25 (b) 0.5

(c) 1.0 (d) 2.0

GATE(EC/1990/2M)

Q.2 The built-in potential (Diffusion Potential) in a p-n junction

(a) Is equal to the difference in the Fermi level of the two sides, expressed in volts

(b) Increases with the increase in the doping levels of the two sides.

(c) Decreases with the increase in temperature

(d) Is equal to the average of the Fermi levels of the two sides.

GATE(EC/1993/2M)

Q.3 The diffusion potential across a P-N junction

(a) decreases with increasing doping concentration

(b) increases with decreasing band gap

(c) does not depend on doping concentration

(d) increases with increase in doping concentrations

GATE(EC/1995/1M)

Q.4 In an abrupt p-n junction, the doping concentrations on the p-side and n–side are $N_A = 9\times10^{16}/cm^3$ and $N_D = 2.7\times10^{17}/cm^3$ respectively. The p-n junction is reverse biased and the total depletion width is 3 μm. The depletion width on the p-side is

(a) 2.7 μm (b) 0.3 μm

(c) 2.25 μm (d) 0.75 μm

GATE(EC/2004/2M)

Q.5 In p^+n junction diode under reverse bias, the magnitude of electric field is maximum at

(a) The edge of the depletion region on the p-side

(b) The edge of the depletion region on the n-side

(c) The p^+n junction

(d) The centre of the depletion region on the n-side

GATE(EC/2007/1M)

Q.6 In a forward biased pn junction diode, the sequence of events that best describes the mechanism of current flow is

(a) injection and subsequent diffusion and recombination of minority carriers

(b) injection and subsequent drift and generation of minority carriers

(c) extraction and subsequent diffusion and generation of minority carriers

(d) extraction and subsequent drift and recombination of minority carriers

GATE(EC/2013/1M)

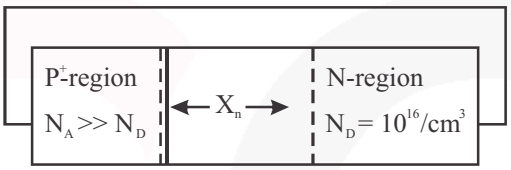
Q.7 The doping concentrations on the p-side and n-side of a silicon diode are 1×10^{16} cm^{-3} and 1×10^{17} cm^{-3}, respectively. A forward bias of 0.3 V is applied to the diode. At T = 300 K, the intrinsic carrier concentration of silicon $n_i = 1.5\times10^{10}$ cm^{-3} and $\frac{kT}{q} = 26\,mV$. The electron concentration at the edge of the depletion region on the p-side is

(a) 2.3×10^{9} cm^{-3} (b) 1×10^{16} cm^{-3}

(c) 1×10^{17} cm^{-3} (d) 2.25×10^{6} cm^{-3}

GATE(EC-I/2014/2M)

Q.8 Consider an abrupt PN junction (at T = 300 K) shown in the figure. The depletion region width X_n on the N-side of the junction is 0.2 μm and the permittivity of silicon (ε_{si}) is 1.044×10^{-12} F/cm. At the junction, the approximate value of the peak electric field (in kV/cm) is_____.



GATE(EC-II/2014/2M)

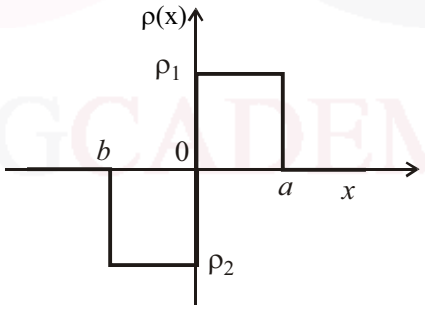
Q.9 When a silicon diode having a doping concentration of $N_A = 9 \times 10^{16}$ cm^{-3} on p-side and $N_D = 1 \times 10^{16}$ cm^{-3} on n - side is reverse biased, the total depletion width is found to be 3 μm. Given that the permittivity of silicon is 1.04×10^{-12} F/cm. F/cm, the depletion width on the p-side and the maximum electric field in the depletion region, respectively, are

(a) 2.7 μm and 2.3×10^{5} V/cm (b) 0.3 μm and 4.15×10^{5} V/cm

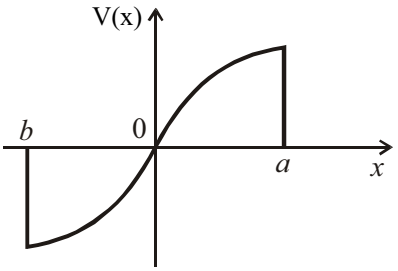
(c) 0.3 μm and 0.42×10^{5} V/cm (d) 2.1 μm and 0.42×10^{5} V/cm

GATE(EC-II/2014/2M)

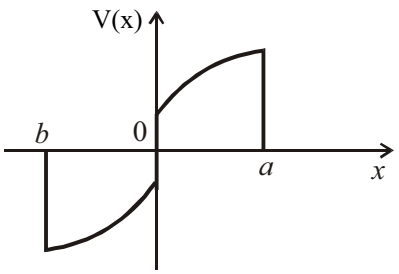
Q.11 Consider the charge profile shown in the figure The resultant potential distribution is best described by



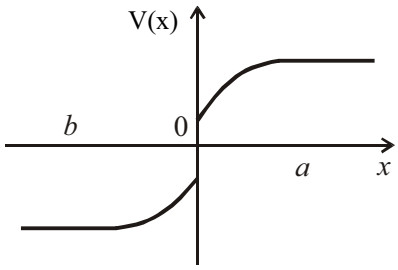
(a)



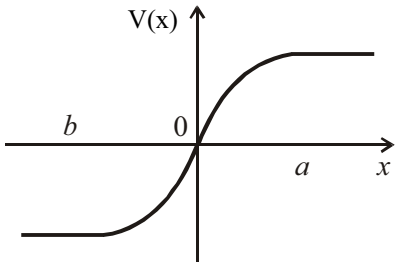
(b)



(c)



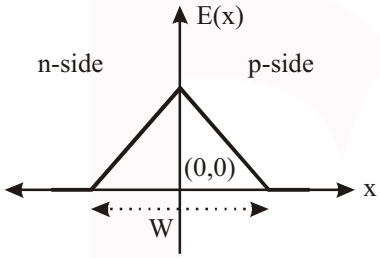
(d)



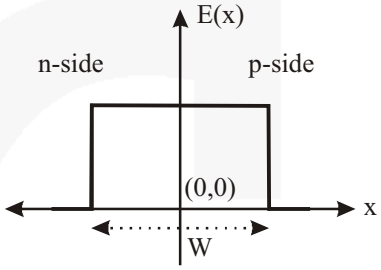
GATE(EC-III/2016/2M)

Q.12 An abrupt pn junction (located at x = 0) is uniformly doped on both p and n sides. The width of the depletion region is W and the electric field variation in the x-direction is E(x). Which of the following figures represents the electric field profile near the pn junction?

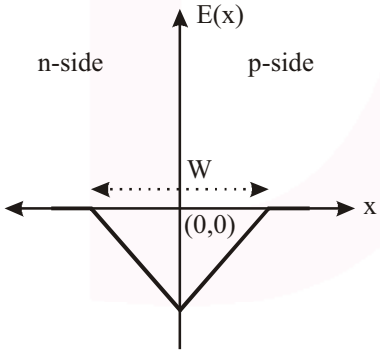
(a)



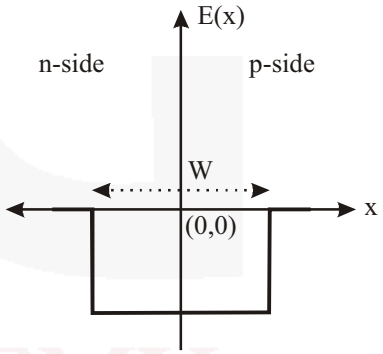
(b)



(c)



(d)



GATE(EC-II/2017/2M)

Q.13 An n^+–n { Silicon device is fabricated with uniform and non-degenerate donor doping concentrations of $N_{D1} = 1\times10^{18}$ cm^{-3} and $N_{D2} = 1\times10^{15}$ cm^{-3} corresponding to the n^+ and n regions respectively. At the operational temperature T, assume complete impurity ionization, kT/q = 25 mV, and intrinsic carrier concentration to be $n_i = 1\times10^{10}$ cm^{-3}. What is the magnitude of the built-in potential of this device?

(a) 0.748V (b) 0.460V

(c) 0.288V (d) 0.173V

GATE(EC-I/2017/1M)

Q.14 In a p-n junction diode at equilibrium, which one of the following statements is NOT TRUE?

(a) The hole and electron diffusion current components are in the same direction.

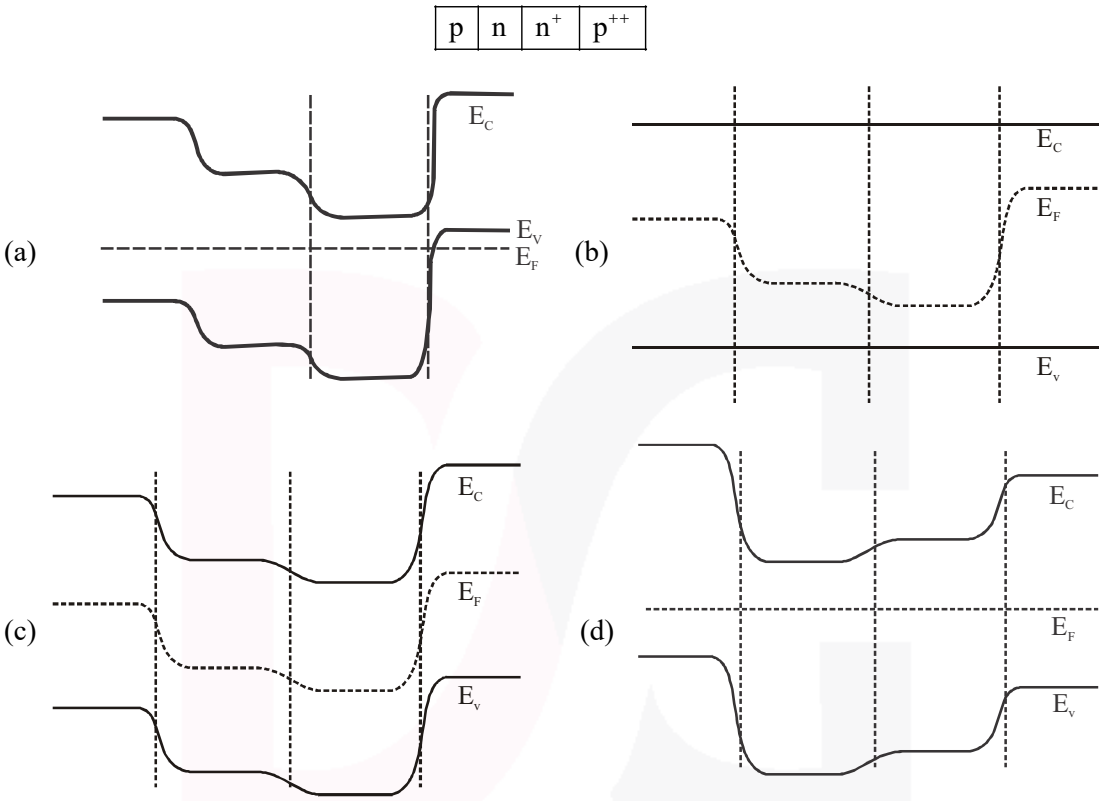
(b) The hole and electron drift current components are in the same direction.

(c) On an average, holes and electrons drift in opposite direction.

(d) On an average, electrons drift and diffuse in the same direction.

GATE(EC/2018/1M)

Q.15 Which one of the following options describes correctly the equilibrium band diagram at T=300 K of a Silicon pnn$^+$ p^{++} configuration shown in the figure?



GATE(EC/2019/1M)

Q.16 A p-n step junction diode with a contact potential of 0.65V has a depletion width of 1 µm at equilibrium. The forward voltage (in volts, correct to two decimal places) at which this width reduces to 0.6 µm is _____.

GATE(EC/2018/1M)

Q.17 The static characteristic of an adequately forward biased p-n junction is a straight line, if the plot is of

(a) log I vs. log V
(b) log I vs. V
(c) I vs. log V
(d) I vs. V

GATE(EC/1996/1M)

Q.18 In an ideal pn junction with an ideality factor of 1 at T=300 K, the magnitude of the magnitude of the reverse-bias voltage required to reach 75% of its reverse saturation current, rounded off to 2 decimal places, is_____mV. [k = 1.38×10^{-23} JK^{-1}, h = 6.625×10^{-34} J-s, q = 1.602×10^{-19}C]

GATE(EC/2019/2M)

Q.19 As the temperature is increased, the voltage across a diode carrying a constant current

(a) Increases.

(b) Decreases.

(c) Remains constant.

(d) May increase or decrease depending upon the doping levels in the junction.

GATE(EE/1999|1M)

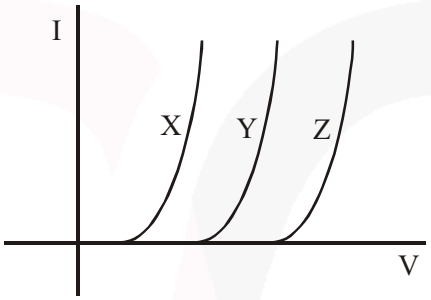
Q.20 For small signal a.c. operation, a practical forward biased diode can be modeled as

(a) a resistance and a capacitance in series (b) an ideal diode and resistance in parallel

(c) a resistance and an ideal diode in series (d) a resistance

GATE(EC/1996/2M)

Q.21 The I-V characteristics of three types of diodes at the room temperature, made of semiconductors X, Y and Z, are shown in the figure. Assume that the diodes are uniformly doped and identical in all respects except their materials. If E_{gX}, E_{gY} and E_{gZ} are the band gaps of X, Y and Z, respectively, then



(a) $E_{gX} > E_{gY} > E_{gZ}$ (b) $E_{gX} = E_{gY} = E_{gZ}$

(c) $E_{gX} < E_{gY} < E_{gZ}$ (d) no relationship among these band gaps exists

GATE(EC-III/2016/1M)

Q.22 A diode whose terminal characteristics are related as $i_D = I_s\left(e^{\frac{V}{V_T}} - 1\right)$ where I_s is the reverse saturation current and V_T is the thermal voltage (= 25 m V), is biased at I_D = 2 mA. Its dynamic resistance is.

(a) 25 ohms (b) 12.5 ohms

(c) 50 ohms (d) 100 ohms

GATE(EE/2000|2M)

Q.23 Which of the following statements is false for a junction diode,

(a) The depletion capacitance increases with increases in the reverse bias

(b) The depletion capacitance decreases with increase in the reverse bias

(c) The diffusion capacitance increases with increase in the forward bias

(d) The diffusion capacitance is much higher than the depletion capacitance when it is forward biased.

GATE(EC/1990/2M)

Q.24 The depletion capacitance, C_T, of an abrupt p-n junction with constant doping on either side varies with reverse bias, V_R, as

(a) $C_T \propto V_R$
(b) $C_T \propto V_R^{-m}$
(c) $C_T \propto V_R^{-1/2}$
(d) $C_T \propto V_R^{-1/3}$

GATE(EC/1995/1M)

Q.25 Compared to a p-n junction with $N_A = N_D = 10^{14}$ cm^{-3}, which one of the following statements is **TRUE** for a p-n junction with $N_A = N_D = 10^{20}$ cm^{-3}?

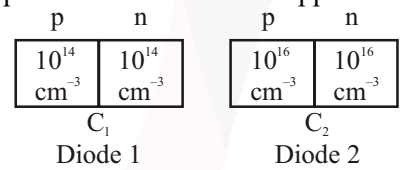
(a) Reverse breakdown voltage is lower and depletion capacitance is lower
(b) Reverse breakdown voltage is higher and depletion capacitance is lower
(c) Reverse breakdown voltage is lower and depletion capacitance is higher
(d) Reverse breakdown voltage is higher and depletion capacitance is higher

GATE(EC/2010/2M)

Q.26 The built-in potential of an abrupt *p-n* junction is 0.75 V. If its junction capacitance (C_j) at a reverse bias (V_R) of 1.25 V is 5 pF, the value of C_j (in pF) when V_R = 7.25 V is .....

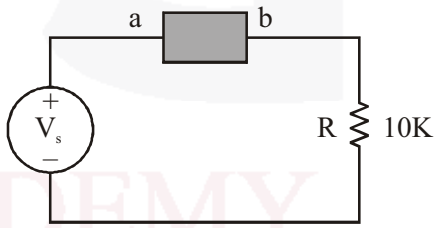
GATE(EC-I/2015/2M)

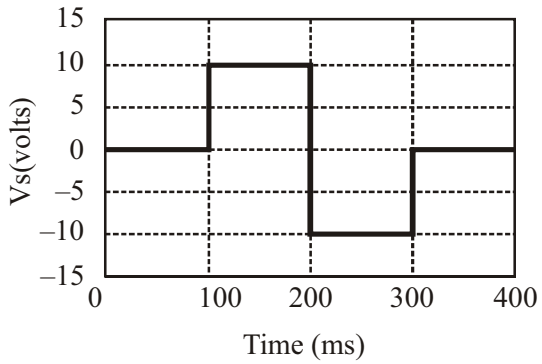
Q.27 As shown, two Silicon (Si) abrupt p-n junction diodes are fabricated with uniform donor doping concentration of $N_{D1} = 10^{14}$ cm^{-3} and $N_{D2} = 10^{16}$ cm^{-3} in the n-regions of the diodes, and uniform acceptor doping concentration of $N_{A1} = 10^{14}$ cm^{-3} and $N_{A2} = 10^{16}$ cm^{-3} in the p-regions of the diodes, respectively. Assuming that the reverse bias voltage is >> built-in potentials of the diodes, the ratio C_2/C_1 of their reverse bias capacitances for the same applied reverse bias, is _____.

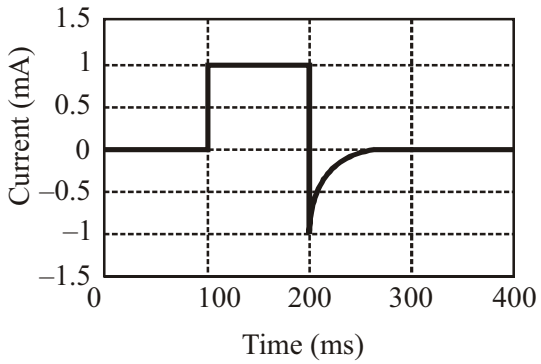


GATE(EC-I/2017/2M)

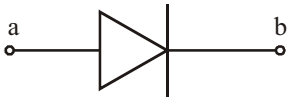
Q.28 The following circuit has a source voltage V_S as shown in the graph . The current through the circuit is also shown.



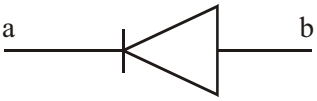


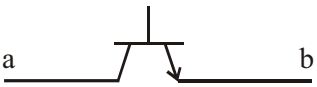


The element connected between a and b could be

(a) 

(b) 

(c) 

(d) 

GATE(EE/2009 | 1 M)

Q.29 A p-n junction in series with a 100 ohms resistor, is forward biased so that a current of 100 mA flows. If the voltage across this combination is instantaneously reversed to 10 V at t = 0, the reverse current that flows through the diode at t = 0 is approximately given by

(a) 0 mA
(b) 100 mA
(c) 200 mA
(d) 50 mA

GATE(EC/1992/2M)

Q.30 A Zener diode works on the principle of

(a) Tunneling of charge carriers across the junction
(b) Thermionic emission
(c) diffusion of charge carriers across the junction
(d) Hopping of charge carriers across the junction

GATE(EC/1995/1M)

Q.31 Consider the following assertions

S1 : For Zener effect to occur, a very abrupt junction is required

S2 : For quantum tunneling to occur, a very narrow energy barrier is required.

Which of the following is correct ?

(a) Only S2 is true
(b) S1 and S2 are both true but S2 is not a reason for S1
(c) S1 and S2 are both true and S2 is a reason for S1
(d) Both S1 and S2 are false.

GATE(EC/2008/2M)

Q.32 A Zener diode, when used in voltage stabilization circuits, is biased in

(a) reverse bias region below the breakdown voltage
(b) reverse breakdown region
(c) forward bias region
(d) forward bias constant current mode

GATE(EC/2011/1M)

Q.33 Consider avalanche breakdown in a silicon p^+ n junction. The n-region is uniformly doped with a donor density N_D. Assume that breakdown occurs when the magnitude of the electric field at any point in the device becomes equal to the critical field E_{crit}. Assume E_{crit} to be independent of N_D. If the built-in voltage of the p^+ n junction is much smaller than the breakdown voltage, V_{BR}, the relationship between V_{BR} and N_D is given by

(a) $V_{BR} \times \sqrt{N_D} = \text{constant}$

(b) $N_D \times \sqrt{V_{BR}} = \text{constant}$

(c) $N_D \times V_{BR} = \text{constant}$

(d) $\frac{N_D}{V_{BR}} = \text{constant}$

GATE(EC-II/2016/2M)

Q.34 The Values of voltage (V_D) across a tunnel - diode corresponding to peak and valley currents are V_p and V_v respectively. The range of tunnel - diode voltage V_D for which the slope of its I-V_D characteristics is negative would be

(a) $V_D < 0$

(b) $0 \le V_D < V_p$

(c) $V_p \le V_D \le V_v$

(d) $V_D \ge V_v$

GATE(EC/2006/1M)

Q.35 A region of negative differential resistance is observed in the current voltage characteristics of a silicon PN junction if

(a) both the P-region and the N-region are heavily doped

(b) the N-region is heavily doped compared to the P-region

(c) the P-region is heavily doped compared to the N-region

(d) an intrinsic silicon region is inserted between the P-region and the N-region

GATE(EC-I/2015/1M)

Q.36 In a forward biased photo diode with increase in incident light intensity, the diode current

(a) Increases

(b) remains constant

(c) Decreases

(d) Remaining constant, the voltage drop across the diode increases.

GATE(EC/1990/2M)

Q.37 Choose proper substitute for X and Y to make the following statement correct Tunnel diode and Avalanche photodiode are operated in X bias and Y bias respectively.

(a) X : reverse, Y : reverse

(b) X : reverse, Y : forward

(c) X : forward, Y : reverse

(d) X : forward, Y : forward

GATE(EC/2003/1M)

Q.38 The quantum efficiency (η) and responsivity (R) at a wavelength λ (in ìm) in a p-i-n photodetector are related by

(a) $R = \frac{\eta \times \lambda}{1.24}$

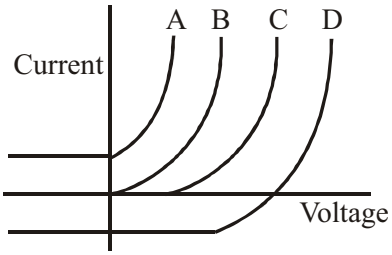
(b) $R = \frac{\lambda}{\eta \times 1.24}$

(c) $R = \frac{1.24 \times \lambda}{\eta}$

(d) $R = \frac{1.24}{\eta \times \lambda}$

GATE(EC/2019/2M)

Q.39 Typical current voltage characteristic of a solar cell is given in the following figure by



(a) curve A (b) curve B

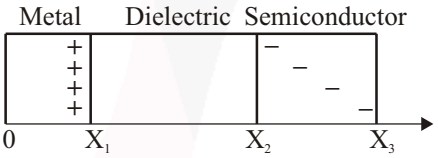
(c) curve C (d) curve D

GATE(EC/1993/2M)

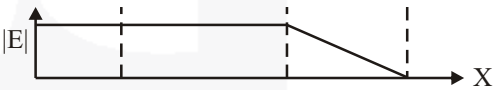
Q.40 A solar cell of area 1.0 cm^2 , operating at 1.0 sun intensity, has a short circuit current of 20 mA, and an open circuit voltage of 0.65 V. Assuming room temperature operation and thermal equivalent voltage of 26mV, the open circuit voltage (in volts, correct to two decimal places) at 0.2 sun intensity is _____.

GATE(EC/2018/2M)

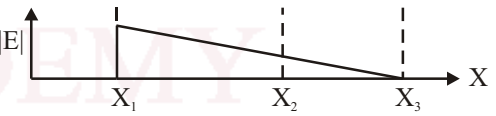
Q.41 The charge distribution in a metal-dielectric-semiconductor specimen is shown in figure. The negative charge density decreases linearly in the semiconductor as shown. The electric field distribution is as shown in



(a) 

(b) 

(c) 

(d) 

GATE(EE/2005 | 2 M)

Q.42 In LED, light is emitted because

(a) recombination of charge carriers takes place (b) diode gets heated up

(c) light falling on the diode gets amplified (d) light gets reflected dur to lens action

GATE(EC/1990/2M)

Q.43 An infra-red LED is usually fabricated from

(a) Ge (b) Si

(c) GaAs (d) GaAsP.

GATE(EC/1992/2M)

Q.44 A particular green LED emits light of wavelength 5490 Å. The energy bandgap of the semiconductor

material used there is (Planck's constant = 6.626×10^{-34} J-s)

(a) 2.26 eV (b) 1.98 eV

(c) 1.17 eV (d) 0.74 eV

GATE(EC/2003/2M)

Q.45 Red (R), Green (G) and Blue (B) Light Emitting Diodes (LEDs) were fabricated using p-n junctions of three different inorganic semiconductors having different band-gaps. The builtin voltages of red, green and blue diodes are V_R, V_G and V_B, respectively. Assume donor and acceptor doping to be the same (N_A and N_D, respectively) in the p and n sides of all the three diodes.

Which one of the following relationships about the built-in voltages is TRUE?

(a) $V_R > V_G > V_B$ (b) $V_R < V_G < V_B$

(c) $V_R = V_G = V_B$ (d) $V_R > V_G < V_B$

GATE(EC/2018/2M)

Q.46 Match List-I (circuit symbols) with List-II (Devices) and select the correct answer using the codes given below the lists

List-I ***List-II***

A. 

1. Light emitting diode

B. 

2. Tunnel diode

C. 

3. Varactor diode

Codes :

	A	**B**	**C**		**A**	**B**	**C**
(a)	1	3	2	(b)	2	3	1
(c)	2	1	3	(d)	1	2	3

GATE(EC/1993/1M)

Q.47 Match items in Group 1 with items in Group 2, most suitably.

Group 1	***Group 2***
P LED	**1.** Heavy doping
Q Avalanche photodiode	**2.** Coherent radiation
R Tunnel diode	**3.** Spontaneous emission
S LASER	**4.** Current gain

(a) P-1,Q-2,R-4,S-3 (b) P-2, Q-3, R-1, S-4

(c) P-3, Q-4, R-1, S-2 (d) P-2, Q-1, R-4, S-3

GATE(EC/2003/2M)

Q.48 Find the correct match between Group-1 and Group-2

Group-1	***Group-2***
E - Varactor diode	1 -Voltage reference

F - PIN diode
G - Zener diode
H - Schottky diode

2 -High - frequency switch
3 -Tuned circuits
4 -Current controlled attenuator

(a) E – 4, F – 2, G – 1, H – 3
(b) E – 2, F – 4, G – 1, H – 3
(c) E – 3, F – 4, G – 1, H – 2
(d) E – 1, F – 3, G – 2, H – 4

GATE(EC/2006/2M)

Q.49 Group I lists four types of p-n junction diodes. Match each device in Group I with one of the options in Group II to indicate the bias condition of that device in its normal mode of operation.

Group-I	***Group-II***
P. Zener Diode	1. Forward bias
Q. Solar cell	2. Reverse bias
R. LASER diode	
S. Avalanche Photodiode.	

(a) P – 1, Q – 2 , R – 1, S – 2
(b) P – 2, Q – 1, R – 1, S – 2
(c) P– 2, Q – 2, R – 1, S – 1
(d) P – 2, Q – 1, R – 2, S – 2

GATE(EC/2007/2M)

Q.50 Which of the following is NOT associated with a p-n junction ?

(a) Junction Capacitance
(b) Charge Storage Capacitance
(c) Depletion Capacitance
(d) Channel Length Modulation

GATE(EC/2008/1M)

Q.51 The correct biasing conditions for typical operation of light emitting diodes, photodiodes, Zener diodes are, respectively

(a) forward bias, reverse bias, reverse bias
(b) reverse bias, reverse bias, forward bias
(c) forward bias, forward bias, reverse bias
(d) reverse bias, forward bias, reverse bias

GATE(IN/2019/1M)

Q.52 A non-ideal diode is biased with a voltage of –0.03 V, and a diode current of I_1 is measured. The thermal voltage is 26 mV and the ideality factor for the diode is 15/13. The voltage, in V, at which the measured current increases to $1.5I_1$ is closest to:

(a) –0.02
(b) –0.09
(c) –1.50
(d) –4.50

GATE(EE/2020/2M)

Q.53 Consider the recombination process via bulk traps in a forward biased pn homojunction diode. The maximum recombination rate is U_{max}. If the electron and the hole capture cross-section are equal, which one of the following is False?

(a) With all other parameters unchanged, U_{max} decreases if the intrinsic carrier density is reduced.
(b) U_{max} occurs at the edges of the depletion region in the device.
(c) U_{max} depends exponentially on the applied bias.
(d) With all other parameters unchanged, U_{max} increases if the thermal velocity of the carriers increases.

GATE(EC/2020/1M)

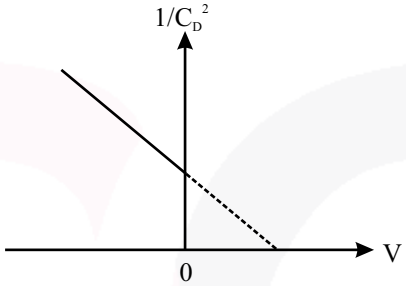
Q.54 A pn junction solar cell of area 1.0 cm^2, illuminated uniformly with 100 mW cm^{-2}, has the following parameters: Efficiency = 15%, open circuit voltage = 0.7 V, fill factor = 0.8, and thickness = 200 µm, The charge of an electron is 1.6×10^{-19} C. The average optical generation rate (in cm^{-3} S^{-1}) is

(a) 0.84×10^{19} (b) 5.57×10^{19}

(c) 1.04×10^{19} (d) 83.60×10^{19}

GATE(EC/2020/2M)

Q.55 A one-sided abrupt pn junction diode has a depletion capacitance C_D of 50 pF at a reverse bias of 0.2 V. The plot of $1/C_D^2$ versus the applied voltage V for this diode is a straight line as shown in the figure below. The slope of the plot is ____ $\times 10^{20}$ F^{-2} V^{-1}.



(a) –5.7 (b) –3.8

(c) –1.2 (d) –0.4

GATE(EC/2020/2M)

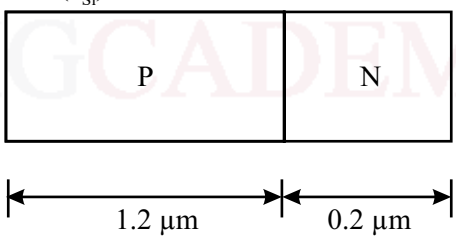
Q.56 A silicon P-N junction is shown in the figure. The doping in the P region is 5×10^{16} cm^{-3} and doping in the N region is 10×10^{16} cm^{-3}. The parameters given are

Built-in voltage (Φ_{bi}) = 0.8 V

Electron charge (q) = 1.6×10^{-19} C

Vacuum permittivity (ε_0) = 8.85×10^{-12} F/m

Relative permittivity of silicon (ε_{Si}) = 12



The magnitude of reverse bias voltage that would completely deplete one of the two regions (P or N) prior to the other {rounded off to one decimal place) is _____V.

GATE(EC/2021/2M)

❐❐❐

ANSWERS & EXPLANATIONS

Q.1 ***Ans.(a)***

On either side of the junction the charge in the depletion layer is same say q_i.

So, the total charge in the depletion layer on the p-side,

$$q_p = (q\,N_A) \times \text{Volume}$$

$$q_p = qN_A \times W_p \times A \qquad \text{.....(i)}$$

Where, A = cross-sectional area

Now, total charge in the depletion layer on the n-side

$$q_n = qN_D \times W_n A \qquad \text{.....(ii)}$$

But, $q_p = q_n$

$$\Rightarrow \quad qN_AW_pA = qN_DW_nA$$

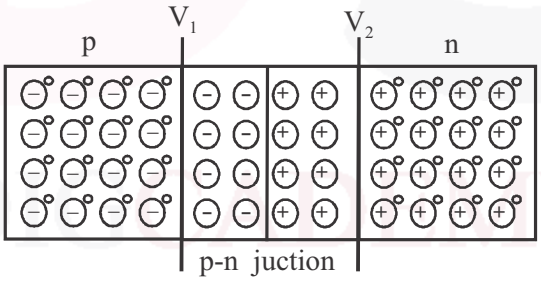
$$\Rightarrow \quad N_AW_p = N_DW_n$$

$$\Rightarrow \quad \frac{W_n}{W_p} = \frac{N_A}{N_D}$$

Given, $N_D = 4\,N_A$

$$\Rightarrow \quad \frac{W_n}{W_p} = \frac{N_A}{4N_A} = \frac{1}{4} = 0.25$$

Q.2 **Ans.(b)**



The built in potential of p-n junction shown above is given by,

$$V_o = (V_2 - V_1)$$

$$= V_T \ell n \frac{p_{po}}{p_{no}} = V_T \ell n \frac{N_A N_D}{n_i^{\,2}}$$

where, p_{po} = concentration of holes on p-side

p_{no} = concentration of holes on n-side

N_A = concentration of acceptor impurities

N_D = concentration of donor impurities

From above equation it is clear the built in potential increases with increase in the concentration of the doping impurities on either sides of the junction but independent of the junction width.

Q.3 ***Ans.(d)***

The diffusion or built-in or contact potential across a p-n junction given by,

$$V_o = \frac{V_T}{q} \ell n \frac{N_A N_D}{n_i^2}$$

Where $N_A \rightarrow$ Acceptor concentration

$N_D \rightarrow$ Donor concentration

$n_i \rightarrow$ Intrinsic concentration

$$\Rightarrow \quad V_o \propto \ell n\, N_A N_D$$

It clear from above relation that diffusion or barrier potential increases with increase in doping concentration.

Q.4 ***Ans.(c)***

Given, $N_A = 9 \times 10^{16}/cm^3$,

$N_D = 2.7 \times 10^{17}/cm^3$

Width of depletion layer, $W = W_p + W_n = 3\ \mu m$

For a p-n diode,

$$N_A W_p = N_D W_n$$

$$\Rightarrow \quad N_A W_p = N_D (W - W_p)$$

$$\Rightarrow \quad (N_A + N_D) W_p = N_D W$$

$$\Rightarrow \quad W_p = \frac{N_D}{N_A + N_D} \times W$$

$$\Rightarrow \quad W_p = \frac{2.7 \times 10^{17}}{(2.7 \times 10^{17} + 9 \times 10^{16})} \times 3 \times 10^{-6}$$

$$\Rightarrow \quad W_p = 2.25\ \mu m$$

Q.5 ***Ans.(c)***

Electric field is always maximum at the junction irrespective of the doping level on n and p side of the junction.

Q.6 ***Ans.(a)***

In a forward biased pn junction the current flows because of minority carrier injection across the junction followed by diffusion of minority carriers near the junction area and then recombination of these minority carriers with majority carriers.

Q.7 ***Ans.(a)***

The electron concentration at the edge of a the depletion region of p-side of a forward biased pn junction is given by,

$$n_p = n_{po} e^{qV_F/kT}$$

Given, $V_F = 0.3\text{ V and } \frac{kT}{q} = 26\text{ mV} = 0.026$

where n_{po} is steady state concentration of electrons on p-side when no bias voltage is applied across the junction. It is given by,

$$n_{po} = \frac{n_i^2}{N_A} = \frac{(1.5\times10^{10})^2}{10^{16}} = 2.25\times10^4\ \text{cm}^{-3}$$

$$\Rightarrow \quad n_p = 2.25\times10^4 \times e^{0.3/0.026} = 2.3\times10^9\ \text{cm}^{-3}$$

Q.8 ***Ans.(30 to 32)***

The electric field at junction of abrupt pn junction is given by,

$$E_{max} = -\frac{qN_D}{\varepsilon}X_n$$

where, X_n is width of space charge on n-side of the junction.

Given, $X_n = 0.2\ \mu\text{m} = 0.2\times 10^{-4}\text{ cm}$

$N_D = 10^{16}\text{ cm}^{-3}$ and

$\varepsilon_{si} = 1.044 \times 10^{-12}\text{ F/cm}$

$$\Rightarrow \quad E_{max} = -\frac{1.6\times10^{-19}\times10^{16}}{1.044\times10^{-12}}\times0.2\times10^{-4} = -30.65\text{ kV/cm}$$

Magnitude of electric field,

$$|E_{max}| = 30.65\text{ kV/cm}$$

Q.9 ***Ans.(b)***

Given, $N_D = 1 \times 10^{16}\text{ cm}^{-3}$

$N_A = 9 \times 10^{16}\text{ cm}^{-3}$

Width of depletion layer,

$$W = W_p + W_n = 3\ \mu\text{m}$$

For a p-n diode,

$$N_A W_p = N_D W_n$$

$$\Rightarrow \quad N_A W_p = N_D(W - W_p)$$

$$\Rightarrow \quad (N_A + N_D)\, W_p = N_D W$$

$$\Rightarrow \quad W_p = \frac{N_D}{N_A + N_D} \times W$$

$$\Rightarrow \quad W_p = \frac{1\times10^{16}}{(1\times10^{16} + 9\times10^{16})} \times 3\times10^{-6}$$

$$\Rightarrow \quad W_p = 0.3\times10^{-4}\ \text{cm} = 0.3\ \mu\text{m}$$

The maximum electric field in the depletion region occurs at junction and it is given by,

$$E_{max} = -\frac{qN_A}{\varepsilon} W_p$$

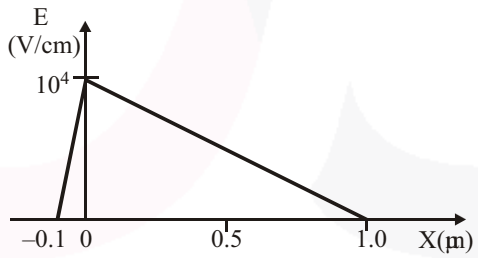
$$\Rightarrow \quad E_{max} = -\frac{1.6\times10^{-19}\times9\times10^{16}}{1.04\times10^{-12}} \times 0.3\times10^{-4}$$

$$\Rightarrow \quad E_{max} = -4.15\times10^{5}\ \text{V/cm}$$

Magnitude of electric field,

$$|E_{max}| = 4.15\times10^{5}\ \text{V/cm}$$

Q.10 ***Ans. (*)***



If the electric field profile in the depletion region of a p-n junction in equilibrium is as shown in the figure above then following conclusions can be drawn,

I. Width of depletion layer on p-side,

$$w_p = 0.1\ \mu\text{m} = 0.1\times10^{-4}\ \text{cm}$$

Width of depletion layer on n-side,

$$w_n = 1.0\ \mu\text{m} = 1\times10^{-4}\ \text{cm}$$

If width of depletion layers is more on n-side then the doping level is more on p-side of the junction.

II. Maximum electric field at junction,

$$E_{max} = 10^4\ \text{V/cm}$$

III. The potential difference across the junction is related to the electric field as under,

$$E = -\frac{dV}{dx}$$

$$\Rightarrow \quad V = -\int E dx = \text{Area under E vs. x curve}$$

$$\Rightarrow \quad V = \frac{1}{2}\times 10^4 \times 0.1\times 10^{-4} + \frac{1}{2}\times 10^4 \times 1\times 10^{-4}$$

$$\Rightarrow \quad V = 0.55\ V$$

Alternatively, the potential difference between the junction can also be obtained by using the relation,

$$E_{max} = \frac{2V}{W}$$

W is total width of the depletion layer.

$$\Rightarrow \quad V = \frac{1}{2}WE_{max} = \frac{1}{2}WE_{max}$$

From the given figure,

$$W = 1 + 0.1 = 1.1\ \mu m = 1.1\times 10^{-4}\ cm$$

$$\Rightarrow \quad V = \frac{1}{2}WE_{max} = \frac{1}{2}\times 1.1\times 10^{-4}\times 10^4 = 0.55V$$

IV. The maximum electric field is related to charge carrier concentration as under,

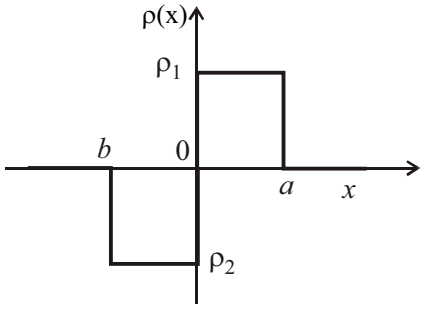
$$E_{max} = \frac{eN_D W_n}{\varepsilon} = \frac{eN_A W_p}{\varepsilon}$$

where, ε is permitivity of the semiconductor material. Here, $\varepsilon$is not given so N_D and N_A can not be computed from the information given in the figure.

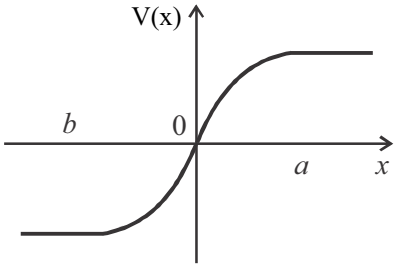
So, none of the given options is correct.

Note : Option (c) given in the answer key is not correct.

Q.11 Ans.(d)



The resultant potential distribution for the charge profile shown above is best described by



Q.12 Ans. (a)

The Possion's equation for space charge region is given by,

$$\Rightarrow \quad \frac{d^2V}{dx^2} = -\frac{\rho_s}{\varepsilon}$$

where V is potential function, ρ_s is space charge density & ε is permitivity of semiconductor material of diode.

Electric field in the space charge region is related to potential function as,

$$E = -\frac{dV}{dx}$$

$$\therefore \quad \frac{d(-E)}{dx} = -\frac{\rho_s}{\varepsilon}$$

$$\Rightarrow \quad \frac{dE}{dx} = \frac{\rho_s}{\varepsilon}$$

Here,
$$\rho_s = q N_D \;;\; \text{for } -W_n \le x \le 0$$
$$= -q N_A \;;\; \text{for } 0 \le x \le W_p$$

Case-I: For $-W_n \le x \le 0$

$$\Rightarrow \quad \frac{dE}{dx} = \frac{q N_D}{\varepsilon}$$

$$\Rightarrow \quad E = \int \frac{q N_D}{\varepsilon} dx + C_1$$

$$\Rightarrow \quad E = \frac{q N_D}{\varepsilon} dx + C_1$$

Let
$$E = 0 \text{ at } x = -W_n$$
$$C_1 = \frac{q N_D W_n}{\varepsilon}$$

$$\Rightarrow \quad E = -\frac{qN_D}{\varepsilon}x + \frac{qN_D}{\varepsilon}W_n \quad ....(i)$$

Case-I: For $0 \le x \le W_p$

$$\therefore \quad E = -\int \frac{qN_A}{\varepsilon}dx + C_2$$

$$\Rightarrow \quad E = -\frac{qN_A}{\varepsilon}x + C_2$$

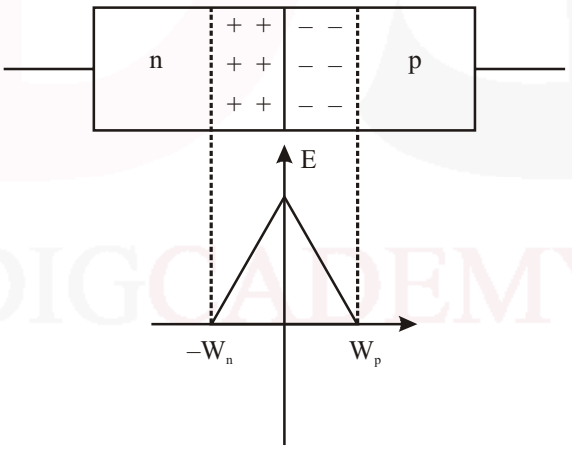
Let $E = 0$ at $x = W_p$

$$\therefore \quad 0 = -\frac{qN_A}{\varepsilon}W_p + C_2$$

$$C_2 = \frac{qN_A}{\varepsilon}W_p$$

$$\Rightarrow \quad E = -\frac{qN_A}{\varepsilon}x + \frac{qN_A}{\varepsilon}W_p \quad ... (ii)$$

The variation in E w.r.t. x can be drawn using equation (i) & (ii) as under,



Q.13 **Ans.(d)**

The built-in potential of unipolar n^+-n junction is given by,

$$V_o = \frac{kT}{q}\ell n\frac{N_D^+}{N_D}$$

Given, $N_D^+ = N_{D1} = 1\times10^{18}\ cm^{-3}$

$N_D = N_{D2} = 1\times10^{15}\ cm^{-3}$

$$\Rightarrow \qquad V_o = 25\ell n\frac{1\times10^{18}}{10^{15}}mV = 0.173V$$

Q.14 Ans.(d)

Facts about a p-n junction diode at equilibrium,

(i) The hole and electron diffusion current components are in the same direction.

(ii) The hole and electron drift current components are in the same direction.

(iii) On an average, holes and electrons drift in opposite direction.

(iv) The direction of diffusion and drift may not be same.

Q.15 Ans.(a)

Facts about Fermi-level,

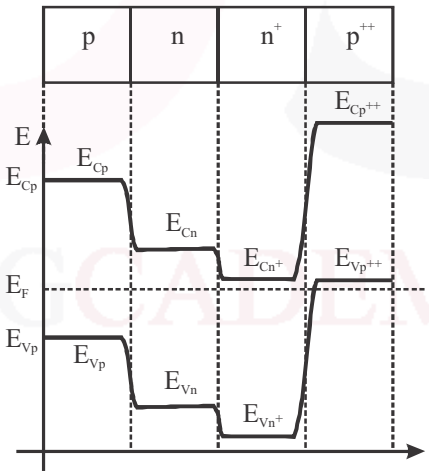
(i) For open circuited pn junctions the Fermi-level is at the same level across all the layer p, n, n^+ & p^{++}.

(ii) Fermi level is closer to valance band in p-type layer and closer to conduction band (CB) in n-layer.

(iii) Fermi level in n^+ layer is more closer to C.B. than n-layer.

(iv) Fermi-level in p^{++} layer is more closes to valence band (VB) than p-layer.

One the basis of above facts the energy band diagram for given pn n^+ p^{++} configuration can be drawn as shown below,



Q.16 ***Ans.(0.40 to 0.43)***

The width of depletion layer,

$$W \propto V_j^{+m}$$

where,

$m = 1/2$; for step abrupt junction

$= 1/3$; for linearly graded junction

$$V_j = V_0 \text{ ; For no biasing voltage}$$
$$= V_0 - V_F \text{ ; For forward biased}$$
$$= V_0 + V_R \text{ ; For reverse biased}$$

V_0 = Barrier potential

V_R = reverse biasing voltage

V_F = forward biasing voltage

Assuming, abrupt junction , we have,

$$W \propto (V_0 - V_F)^{+1/2}$$

$$\Rightarrow \quad \frac{W_2}{W_1} = \left(\frac{V_o - V_F}{V_o}\right)^{1/2},$$

$$\Rightarrow \quad \frac{0.6}{1} = \left(\frac{0.65 - V_F}{0.65}\right)^{1/2}$$

$$\Rightarrow \quad V_F = 0.42 \text{ V}$$

Q.17 Ans.(b)

The diode current equation is given by

$$I = I_o\left[e^{\frac{V_D}{\eta V_T}} - 1\right]$$

where, V_D = voltage across the diode

V_T = Thermal voltage = $\frac{T}{11600}$

$\eta = 1$ for Ge

$= 2$ for Si

$$\Rightarrow \quad I + I_o = I_o e^{\frac{V_D}{\eta V_T}}$$

Since forward diode current , $I_D >> I_S$, therefore,

$$I + I_o \approx I$$

$$\Rightarrow \quad I = I_o e^{\frac{V_D}{\eta V_T}}$$

Taking log on both the sides, we have

$$\log_e I = \log_e I_o + \frac{V}{\eta V_T}$$

$$y = c + m.x \qquad \text{.....(i)}$$

$y = \log_e I$, $x = V$, $c = \log_e I_o$ and

$$m = \frac{1}{\eta V_T}$$

Equation 1 represents equation of a straight line between $\log_e I$ and V. It is called Logarithmic characteristic of diode.

Note :- *The logarithmic characteristics of diode are applicable for small values of diode current. For higher value of diode current I increases linearly with V and diodes behaves like a resistance.*

Q.18 Ans.(34.00 to 38.00)

The current through a forward biased diode is given by,

$$I = I_o\left(e^{\frac{V_D}{\eta V_T}} - 1\right)$$

Under reverse bias, $V_D = -V_R$ and I is negative.

$$\therefore \quad I = -I_o\left(e^{-\frac{V_R}{\eta V_T}} - 1\right)$$

Given, $\eta = 1$, $V_T = \frac{kT}{q} = \frac{T}{11600}$

At 300 K, $V_T = \frac{300}{11600} = 0.02586$

Let $V_R = V_{R1}$ when $I = 0.75 I_o$ at

$$\therefore \quad 0.75\, I_o = -I_o\left(e^{-\frac{V_{R1}}{1\times 0.02586}} - 1\right)$$

$$\Rightarrow \quad V_{R1} = 35.849 \text{ mV}$$

Q.19 Ans.(b)

The variation of voltage across a diode is given by,

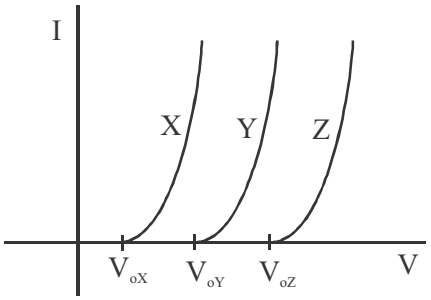
$$\frac{dV}{dT} = -2.5 \text{ mV/°C}$$

Thus the voltage across the diode decreases when the temperature is increased.

Q.20 Ans.(d)

For small signal a.c. operation, a practical forward biased diode can be modeled as a resistance.

Q.21 **Ans. (*c*)**



From the given I-V characteristics, it is observed that potential barrier of semiconductors X,Y & Z is related as under,

$$V_{oX} < V_{oY} < V_{oZ}$$

The band gap of a semiconductor is directly proportional to the barrier potential as under,

$$E_g = qV_o$$

$$\Rightarrow \quad E_g \propto V_o$$

$$\Rightarrow \quad E_{gX} < E_{gY} < E_{gZ}$$

Q.22 Ans.(b)

The dynamic resistance,

$$r_d = \frac{\eta V_T}{I_D} = \frac{\eta \times 25 \times 10^{-3}}{2 \times 10^{-3}}$$

Assuming, $\eta = 1$,

then, $$r_d = \frac{1 \times 25 \times 10^{-3}}{2 \times 10^{-3}} = 12.5 \text{ ohms}$$

Note:- *The diode current equation is given by*

$$I_D = I_o\left[e^{\frac{V}{\eta V_T}} - 1\right]$$

The dynamic or incremental conductance of diode is given by,

$$g = \frac{dI_D}{dV} = \frac{d}{dV}\left[I_o\left(e^{\frac{V}{\eta V_T}} - 1\right)\right]$$

$$\Rightarrow \quad g = \frac{I_o e^{\frac{V}{\eta V_T}}}{\eta V_T} = \frac{I_D + I_o}{\eta V_T}$$

Since forward diode current , $I_D >> I_o$, therefore,

$$I_D + I_o \approx I_D$$

$$\Rightarrow \qquad g = \frac{I_D}{\eta V_T}$$

dynamic resistance,

$$\Rightarrow \qquad r_d = \frac{1}{g} = \frac{\eta V_T}{I_D}$$

Q.23 Ans.(a)

I. Depletion layer Capacitance :

The depletion layer capacitance of a junction diode is given,

$$C_T = \frac{\varepsilon A}{W} \qquad \text{.....(i)}$$

where, ε = permitivity

A = area of cross-section of junction

W = width of the depletion layer

The width of depletion layer is given by,

$$W = \sqrt{\left(\frac{2\varepsilon}{q}\right)\left(\frac{1}{N_A}+\frac{1}{N_D}\right)V_j} \qquad \text{.....(ii)}$$

where, $V_j = V_0$; For no biasing voltage

$= V_0 - V_F$; For forward bias

$= V_0 + V_R$; For reverse bias

V_0 = Barrier potential

V_R = reverse biasing voltage

V_F = forward biasing voltage

N_D = concentration of donor impurity

N_A = concentration of acceptor impurity

From equations (i) & (ii) the depletion capacitance under reverse biasing mode,

$$C_T = \frac{\varepsilon A}{\sqrt{\left(\frac{2\varepsilon}{q}\right)\left(\frac{1}{N_A}+\frac{1}{N_D}\right)(V_o+V_R)}}$$

It is clear from equation that the depletion capacitance decreases with increase in applied reverse voltage.

Note:- *Depletion capacitance is also known as transition capacitance or space charge capacitance.*

II. Diffusion capacitance of diode :

The diffusion capacitance of diode is given by,

$$C_D = \frac{\tau I_D}{\eta V_T}$$

where, τ = average life time of minority carriers in n-region

I_D = diode current

V_T = thermal voltage

η = 1 for Ge

= 2 for Si

The diode current is given by,

$$I = I_o\left[e^{\frac{V}{\eta V_T}} - 1\right] \simeq I_o e^{\frac{V}{\eta V_T}}$$

where, V = biasing voltage across the diode

V_T = Thermal voltage = $\frac{T}{11600}$

η = 1 for Ge

= 2 for Si

Then, diffusion capacitance,

$$\Rightarrow \quad C_D = \frac{\tau I_o e^{\frac{V_f}{\eta V_T}}}{\eta V_T}$$

$$\Rightarrow \quad C_D \propto e^{\frac{V}{\eta V_T}}$$

So, diffusion capacitance increases exponentially with increase in forward bias voltage.

Note:- *Diffusion capacitance is also known as storage capacitance.*

III. Comparison of C_D & C_T:

Diffusion capacitance is much higher than depletion capacitance under forward biased condition and depletion capacitance is much higher than the diffusion capacitance when the diode is reverse biased.

Thus, statement of option (a) is false.

Q.24 Ans.(c)

The depletion layer capacitance of a junction diode is given,

$$C_T = \frac{\varepsilon A}{W} \qquad \text{.....(i)}$$

where, ε = permitivity

A = area of cross-Section of junction

W = width of the depletion layer

The width of depletion layer,

$$W \propto V_j^m$$

$$\Rightarrow \quad C_T \propto V_j^{-m}$$

where, $m = 1/2$; for step graded or abrupt junction

$= 1/3$; for linearly graded junction

$V_j = V_0$; For no biasing voltage

$= V_0 - V_F$; For forward biased

$= V_0 + V_R$; For reverse biased

V_0 = Barrier potential

V_R = reverse biasing voltage

V_F = forward biasing voltage

Therefore, for abrupt junction,

$$C_T \propto (V_0 + V_R)^{-1/2}$$

For large reverse biasing voltage,

$$V_0 + V_R \approx V_R$$

$$\Rightarrow \quad C_T \propto V_R^{-1/2}$$

Q.25 Ans.(c)

Depletion layer capacitance of diode is given by

$$C_T = \frac{\varepsilon A}{W}$$

where, A is area of cross-section of junction and W is width of depletion layer

The width of depletion layer of pn junction is given by,

$$W = \sqrt{\frac{2\varepsilon}{q}\left[\frac{1}{N_D} + \frac{1}{N_A}\right]V_j}$$

Where,

V_j = Junction voltage.

N_D = Donor concentration.

N_A = Acceptor concentration

When impurity concentration is increased the depletion layer width reduces which in turn increases the depletion layer capacitance.

The electric field intensity in depletion layer is given by,

$$E \propto \frac{V_j}{W}$$

So, the electric field intensity in depletion layer increases with decreases in depletion layer width for fixed junction voltage. Hence breakdown voltage reduces with increase in doping concentration. For example a Zener breakdown occurs at lower voltage in heavily doped diode than avalanche multiplication which occurs at higher voltage in lightly doped diode.

Q.26 **Ans. 2.4 to 2.6**

The depletion layer capacitance of a junction diode is given,

$$C_j = \frac{\varepsilon A}{W} \qquad \text{.....(i)}$$

Where, ε = permitivity

A = area of cross-section of junction

W = width of the depletion layer

The width of depletion layer,

$$W \propto V_j^{+m}$$

$$\Rightarrow \quad C_j \propto V_j^{-m}$$

where, $m = 1/2$ for step graded or abrupt junction

$= 1/3$ for linearly graded junction

$V_j = V_0$; For no biasing voltage

$= V_0 - V_F$;For forward biased

$= V_0 + V_R$;For reverse biased

V_0 = Barrier potential or built in potential

V_R = reverse biasing voltage

V_F = forward biasing voltage

Therefore, for abrupt junction,

$$C_j \propto (V_0 + V_R)^{-1/2}$$

$$\Rightarrow \quad \frac{C_{j2}}{C_{j1}} = \frac{(V_0 + V_{R2})^{-1/2}}{(V_0 + V_{R1})^{-1/2}}$$

$$\Rightarrow \quad C_{j2} = \frac{(V_0 + V_{R2})^{-1/2}}{(V_0 + V_{R1})^{-1/2}} \times C_{j1}$$

$$\Rightarrow \quad C_{j2} = \frac{(0.75 + 7.25)^{-1/2}}{(0.75 + 1.25)^{-1/2}} \times 5 = 2.5 \text{ pF}$$

Q.27 Ans. : 10.0

The depletion layer capacitance of a junction diode is given,

$$C_j = \frac{\varepsilon A}{W} \qquad \text{.....(i)}$$

where, ε = permitivity

A = area of cross-section of junction

W = width of the depletion layer

The width of depletion layer,

$$W = \sqrt{\frac{2\varepsilon}{q}\left[\frac{1}{N_D}+\frac{1}{N_A}\right]V_j}$$

$$W \propto \sqrt{\left[\frac{N_A+N_D}{N_A N_D}\right]V_j}$$

$$\Rightarrow \quad C_j \propto \left[\frac{N_A+N_D}{N_A N_D}\times V_j\right]^{-1/2}$$

where, $V_j = V_0 + V_R$;For reverse biased

V_0 = Barrier potential or built in potential

V_R = reverse biasing voltage

Given, $V_R >> V_0$

$\therefore \quad V_j \approx V_R$

Therefore, for abrupt junctions,

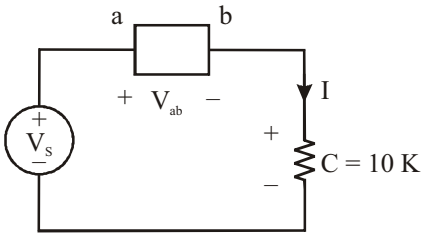
$$C_j \propto \left[\frac{N_A+N_D}{N_A N_D}\times V_R\right]^{-1/2}$$

$$\Rightarrow \quad \frac{C_{j2}}{C_{j1}} = \frac{\left[\frac{N_{A2}+N_{D2}}{N_{A2}N_{D2}}\times V_{R2}\right]^{-1/2}}{\left[\frac{N_{A1}+N_{D1}}{N_{A1}N_{D1}}\times V_{R1}\right]^{-1/2}}$$

Given, $V_{R2} = V_{R1}$

$$\Rightarrow \quad \frac{C_{j2}}{C_{j1}} = \frac{\left[\frac{10^{16}+10^{16}}{10^{16}\times 10^{16}}\right]^{-1/2}}{\left[\frac{10^{14}+10^{14}}{10^{14}\times 10^{14}}\right]^{-1/2}} = 10 = 10$$

Q.28 **Ans.(a)**



Case-I : Positive half cycle of V_s

During positive half cycle of V_S , I = 1 mA, V_S = 10 V

KVL in circuit given, $V_S - V_{ab} - IR = 0$

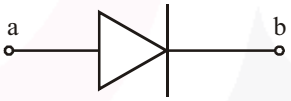
$$\Rightarrow \quad V_{ab} = V_S - IR = 10 - 10 \times 10^3 \times 10^{-3} = 0 \text{ V}$$

As V_{ab} = 0 V during positive half cycle of input voltage so the element between a and b behaves as a short circuit during positive half cycle.

Case-II: Negative half cycle of V_S

During negative half cycle the current through element is negative and maximum initially and then reduces exponentially. This behaviour is similar to series RC circuit connected to a dc source. So, element behaves as a capacitive element during negative half cycle.

Conclusion : A diode behaves as short circuit when it is forward biased and as a capacitor when reverse biased so, the element between a and b must a diode with 'a' connected to anode and 'b' connected to cathode as under,



Q.29 ***Ans.(b)***

When the voltage across a diode is suddenly applied in reverse direction the current in diode starts flowing in reverse direction because of excess minority carrier. The magnitude of current in reverse direction will be controlled by load resistance and reverse voltage. The reverse current at t = 0 will be,

$$I_R = -V_R / R_L = -10 / 100 = -100 \text{ mA}$$

Thus the magnitude of reverse current at t = 0 will is same as magnitude of forward current at t = 0 but in reverse direction.

Q.30 ***Ans.(a)***

A Zener diode works on the principle of tunneling of charge carriers across the junction which leads the junction to breakdown.

Q.31 ***Ans.(c)***

For Zener effect to occur, a very abrupt junction is required because for quantum tunneling to occur, a very narrow energy barrier is required. Therefore, both S1 and S2 are both true and S2 is a reason for S1.

Q.32 ***Ans.(a)***

A Zener diode, when used in voltage stabilization circuits is biased in reverse breakdown region i.e. third quadrant of vi-characteristics of diode.

Q.33 ***Ans. (c)***

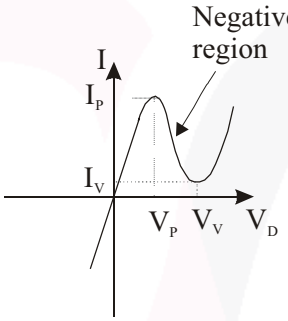
The breakdown voltage of p^+n junction diode is given by,

$$V_{BR} = \frac{\varepsilon E_{cr}^{\ 2}}{2qN_D}$$

$$\Rightarrow \quad N_D \times V_{BR} = \text{constant}$$

Q.34 ***Ans.(c)***

The V-l characteristic of a tunnel diode has negative resistance region and it is best represented as,



The range of tunnel - diode voltage V_D for which the slope of its I-V_D characteristics is negative would be $V_p \leq V_D \leq V_v$

Q.35 ***Ans. (a)***

A region of negative differential resistance is observed in the current voltage characteristics of a silicon PN junction if both the P-region and the N-region are heavily doped.

Q.36 ***Ans.(a)***

In semiconductor photo diode the number of new holes and electrons pair generated is proportional to the number of incident photons. So, diode current will increase with increase in intensity of light.

Q.37 ***Ans.(c)***

A tunnel diode works in negative resistance region under forward biased mode and a Avalanche photodiode work in reverse biased mode.

Q.38 Ans.(a)

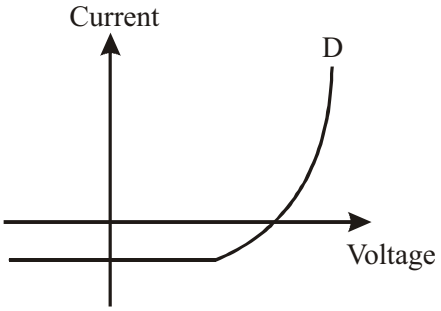
The responsivity of a photodetector is given by,

$$R = \frac{\eta\lambda}{1.24}$$

where η is is quantum efficiency and λ is wave length of incident light in μm.

Q.39 ***Ans.(d)***

Typical current voltage characteristic of a solar cell is given in the following figure by



Note :- *A solar cell operates in fourth quadrant of v-i characteristic.*

Q.40 **Ans.(0.59 to 0.63)**

The open circuited or photo voltage of a solar cell is given by,

$$V_{oc} = \eta V_T \ln\left(1+\frac{I_{sc}}{I_o}\right)$$

Given, $V_{oc} = 0.65\ V,\ I_{sc} = 20\ mA$

$V_T = 26mV$, As η is not specified so take it 1.

$$\Rightarrow \quad 0.65 = 26\times10^{-3}\ln\left(1+\frac{20\times10^{-3}}{I_o}\right)$$

$$\Rightarrow \quad I_o = 0.277\times10^{-12}\ A$$

The photocurrent of a solar cell is directly proportional to the intensity of light falling on it. If intensity of light is decreased from 1 sun intensity to 0.2 that means new intensity has become $1/5^{th}$ of initial intensity then the photo current also becomes $1/5^{th}$ of its initial value. If initial photo current density is 20 mA then the new photocurrent will 0.2×20 mA.

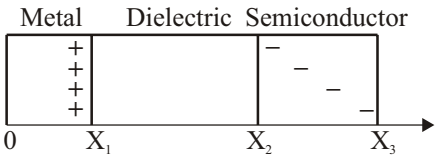
Then the open circuited voltage becomes as under,

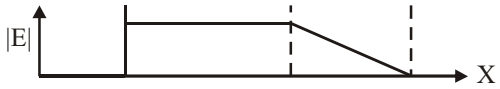
$$V_{oc} = 26\times10^{-3}\ln\left(1+\frac{0.2\times20\times10^{-3}}{0.277\times10^{-12}}\right) = 0.608\ V$$

Q.41 ***Ans.(a)***

In the metal, the electric field will be zero. In dielectric material, the electric field will remain constant through out and in semiconductor due to the distribution of negative charge, the electrical field will decrease linearly.

Therefore, the electric field distribution in metal-dielectric-semiconductor specimen will be as shown below.





Q.42 Ans.(a)

In LED, light is emitted because of recombination of charge carriers. When an electron jumps from the higher energy level i.e. C.B. to lower energy level i.e. V.B. then it emits radiation.

Q.43 Ans.(c)

An infra-red LED is usually fabricated from GaAs.

Q.44 Ans.(a)

Given, Wavelength of light emitted by LED,

$$\lambda = 5490 \text{ Å}$$

The wavelength of light emitted by LED is given by,

$$\lambda = \frac{12400}{E_g} \text{Å}$$

where, E_g is energy gap in eV

$$\Rightarrow \quad E_g = \frac{12400}{\lambda} \text{ eV}$$

$$\Rightarrow \quad E_g = \frac{12400}{5490} = 2.26\text{eV}$$

Q.45 Ans.(b)

The wavelength of light emitted by LED is given by,

$$\lambda = \frac{hc}{E_g}$$

Where, E_g is energy gap in eV.

$$\Rightarrow \quad E_g = \frac{hc}{\lambda}$$

$$\Rightarrow \quad E_g \propto \frac{1}{\lambda}$$

So, the semiconductor material emitting light of smaller wavelength larger band gap. The band gap of a semiconductor is directly proportional to the built-in potential. Therefore, semiconductor emitting light of smaller wavelength have higher built-in potential. In electromagnetic spectrum of light the wavelength of Red (R), Green (G) and Blue light has following relation,

$$\lambda_R > \lambda_G > \lambda_B$$

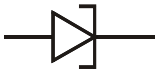
$\therefore$ Relation in built-in potential of semiconductors emitting red, green and blue light will be,

$$V_R < V_G < V_B$$

Q.46 Ans.(a)

A. Symbol of LED : 

B. Symbol of Varactor diode : 

C. Symbol of tunnel diode : 

Q.47 Ans.(c)

P LED gives spontaneous emission.

Q Avalanche photodiode provides current gain

R Tunnel diode has heavy doping level.

S LASER emits coherent radiation.

Q.48 Ans.(c)

I. Varactor diode is used in tuned circuits.

II. PIN diode can be used as Current controlled attenuator

III. Zener diode is used for voltage reference

IV. Schottky diode can be used as High - frequency switch

Q.49 Ans.(b)

P. Zener Diode works under reverse bias mode in third quadrant of v– i characteristics.

Q. Solar cell works under forward biased mode in fourth quadrant of v– i characteristics.

R. LASER diode works under forward bias mode in first quadrant of v-i characteristics.

S. Avalanche Photodiode works under reverse bias mode in third quadrant of v-i characteristics.

Q.50 Ans.(d)

Parameters of pn junction,

i. Junction Capacitance

ii. Charge Storage Capacitance

iii. Depletion Capacitance

The channel length modulation is not associated with a pn junction.

Q.51 Ans.(a)

1. An LED works in forward bias mode.
2. A photo diode works in revere bias mode.
3. A Zener diode works in reverse bias mode.

Q.52 Ans(b)

The current through a diode is given by

$$I = I_o\left(e^{\frac{V_D}{\eta V_T}} - 1\right)$$

Where I_o is reverse saturation current, V_D is voltage across the diode, η is ideality factor and V_T is thermal voltage.

When $V_D = -0.03$ V and $I = I_1$

$$\Rightarrow \quad I_1 = I_o\left(e^{\frac{-0.03}{\frac{15}{13}\times 0.026}} - 1\right) = -0.632\, I_o$$

When $I = 1.5 I_1 = -1.5 \times 0.632\, I_o$

$$\Rightarrow \quad -1.5 \times 0.632\, I_o = I_o\left(e^{\frac{V_D}{\frac{15}{13}\times 0.026}} - 1\right)$$

$$\Rightarrow \quad 1 - 1.5 \times 0.632 = e^{\frac{13 V_D}{15\times 0.026}}$$

$$\Rightarrow \quad V_D = -0.0888 \text{ V}$$

Q.53 ***Ans(b)***

Facts about maximum recombination rate is U_{max} via bulk traps in a forward biased pn homojunction diode,

i. With all other parameters unchanged, U_{max} decreases if the intrinsic carrier density is reduced.
ii. U_{max} depends exponentially on the applied bias.
iii. With all other parameters unchanged, U_{max} increases if the thermal velocity of the carriers increases.

Q.54 ***Ans(a)***

Given, $V_{oc} = 0.7$ V, Area of cell = 1.0 cm^2, Thickness of cell = 200 μm, Light intensity = 100 mW cm^{-2}, Fill factor = 0.8 mW cm^{-2}.

Input optical power, $P_{in} = 100 \times 10^{-3} \times 1 = 100$ mW

Output power, $P_{out} = \eta P_{in} = 0.15 \times 100 \text{ W} = 15\text{mW}$

Fill factor of solar cell,

$$FF = \frac{P_{out}}{V_{oc} I_{sc}}$$

$$\Rightarrow \quad I_{sc} = \frac{P_{out}}{V_{oc} \times FF} = \frac{15}{0.7 \times 0.8}\text{mA}$$

The short circuit current of solar cell in terms of optical generation rate can be given by,

$$I_{sc} = g_{op} \times \text{volume} \times q$$

$$\Rightarrow \quad \frac{15}{0.7\times 0.8}\times 10^{-3} = g_{op} \times 200\times 10^{-6}\times 1\times 10^{-4}\times 1.6\times 10^{-19}$$

or $g_{op} = 0.837 \times 10^{25}\ m^{-3}\ s^{-1} = 0.837 \times 10^{19}\ cm^{-3}\ s^{-1}$

Q.55 Ans(b)

The depletion layer capacitance of a diode is given by,

$$C_o = \frac{\varepsilon A}{W}$$

Where, $W = \sqrt{\frac{2\varepsilon}{q}\cdot\left(\frac{1}{N_A}+\frac{1}{N_D}\right)\cdot(V_o - V_F)}$

Where V_o is built in potential and V_F forward bias voltage.

Let given abrupt P^n junction is with $N_D >> N_A$,

$$\frac{1}{N_A}+\frac{1}{N_D} \approx \frac{1}{N_A}$$

$$\Rightarrow \quad W = \sqrt{\frac{2\varepsilon}{q}\cdot\frac{1}{N_A}\cdot(V_o - V_F)}$$

$$\Rightarrow \quad C_D = \frac{\varepsilon A}{\sqrt{\frac{2\varepsilon}{q}\cdot\frac{1}{N_A}(V_o - V_F)}}$$

$$\Rightarrow \quad \frac{1}{C_D^{\,2}} = \frac{1}{A^2\varepsilon}\cdot\frac{2}{q}\cdot\frac{1}{N_A}(V_o - V_F) \qquad ...(i)$$

$$\frac{1}{C_D^{\,2}} = -\frac{1}{A^2\varepsilon}\cdot\frac{2}{q}\cdot\frac{1}{N_A}V_F + \frac{1}{A^2\varepsilon}\cdot\frac{2}{q}\cdot\frac{1}{N_A}\cdot V_o \qquad .....(ii)$$

Let built in potential of diode is diode is 0.8V

Then at reverse bias voltage of 0.2 V

$V_F = -0.2$ V and $C_D = 50$ pF, we have,

$$\frac{1}{(50\times10^{-12})^2} = \frac{1}{A}\cdot\frac{2}{q}\cdot\frac{1}{N}(0.8+0.2)$$

$$\Rightarrow \quad \frac{1}{A^2\varepsilon}\cdot\frac{2}{q}\cdot\frac{1}{N_A} = 4\times10^{20}\ F^{-2}\ V^{-1}$$

Equation (ii) can be written in term of equation of straight line as under

$$y = mx + c$$

Where, $y = \frac{1}{C_D^{\,2}}$, $m = -\frac{1}{A^2\varepsilon}\cdot\frac{2}{q}\cdot\frac{1}{N_A} = \text{slope}$, $x = V_F$

and $$c = \frac{1}{A^2\varepsilon}\cdot\frac{2}{q}\cdot\frac{1}{N_A}\cdot V_o$$

$\therefore$ Slope of $\frac{1}{C_D^{\,2}}$ v_s V curve is,

$$-\frac{1}{A^2\varepsilon}\cdot\frac{2}{q}\cdot\frac{1}{N_A} = -4\times10^{20}\ F^2\ V^{-1}$$

So, nearest answer is option (b).

Q.56 Ans.(8.1 to 8.4)

Given, $$N_A = 5\times10^{16}\ cm^{-3}$$
$$N_D = 10\times10^{16}\ cm^{-3}$$

The N region is completely depleted when width of depletion layer on n-side becomes equal to 0.2 μm.

$$W_n = 0.2\ \mu m$$

Total width of depletion layer is related with depletion layer width an n-side as,

$$W_n = \frac{N_A}{N_A+N_D}\cdot W$$

$\Rightarrow$ $$W = \frac{N_A+N_D}{N_A}\times W_n = \frac{5\times10^{16}+10\times10^{16}}{5\times10^{16}}\times0.2\mu m$$

$\Rightarrow$ $$W = 3\times0.2\ \mu m = 0.6\ \mu m = 0.6\times10^{-4}\ cm$$

The width of depletion layer of a diode is given by,

$$W = \sqrt{\frac{2\varepsilon}{q}\left[\frac{1}{N_A}+\frac{1}{N_D}\right](V_{bi}+V_R)}$$

When $V_{bi} = \phi_{bi}$ = built in potential of junction
V_R = Reverse biasing voltage
$\varepsilon = \varepsilon_o\,\varepsilon_{rs}$
$\varepsilon_o = 8.85\times10^{-12}$ F/m $= 8.85\times10^{-14}$ F/cm, $\varepsilon_{rs} = 12$

The region n will be completely covered by depletion layer if W be comes 0.6 μm.

$$\Rightarrow \quad 0.6 \times 10^{-4} = \sqrt{\frac{2 \times 8.85 \times 10^{-14} \times 12}{1.6 \times 10^{-19}} \left[\frac{1}{5 \times 10^{16}} + \frac{1}{10 \times 10^{16}} \right] \times \left(0.8 + V_R \right)}$$

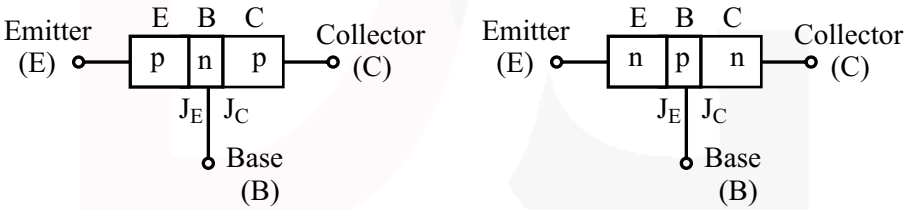
$$\Rightarrow \quad V_R = 8.24 \text{ V}$$

❐❐❐

Ch 3 Bipolar Junction Transistors

3.1 Construction of BJT

Bipolar junction transistor (BJT) is a bipolar, three layer, three terminal and two junctions device. The three layers of BJT are called emitter, base and collector. Corresponding terminals of emitter, base and collector layers are called emitter (E), base (B) and collector (C) terminals, respectively. The junction between emitter and base layers is called emitter junction (J_E) and junction between base and collector layers is called collector junction (J_C). The BJT can be either pnp type in which one n-layer is sandwiched between two p-layers or npn type in which one p-layer is sandwiched between two n-layers as shown in Fig.1. The npn transistor is preferred over pnp transistor because of higher mobility of electrons as compared to mobility of holes.



(a) pnp transistor (b) npn transistor

Fig. 1 Layer diagram of BJT (a) pnp transistor (b) npn transistor

The symbols of pnp and npn transistors are as shown in Fig. 2. The direction of arrow sign on emitter terminal indicates the direction of emitter current in the BJT.

(a) pnp transistor (b) npn transistor

Fig. 2 Symbols of BJT (a) pnp transistor (b) npn transistor

Emitter junction is step graded and collector junction is linearly graded. The current in BJT is contributed by both electrons and holes due to which it is called a bipolar device. The doping

level of emitter is highest i.e. emitter is heavily doped, base is moderately doped and collector of BJT has smallest doping level. The typical doping concentrations of emitter, base and collector is of order of $N_E = 10^{19}$,$N_B = 10^{17}$and $N_C = 10^{15}$ per cm^{-3}, respectively. The width of depletion layer at the emitter junction is narrow due to high doping concentration of emitter and most of it lies in the base region of the transistor. Since emitter of BJT has highest doping level, therefore, it has highest conductivity and lowest resistivity. The base region being narrow with low doping level so it has high resistivity and less conductivity. Physical size of collector region is largest so that sufficient heat is dissipated from the reverse biased collector junction. Width of base region is much smaller than the diffusion length of minority carriers for operation of BJT as an amplifier.

A BJT can be used either as an amplifier or as a switch. When BJT is used as an amplifier, the emitter junction is forward biased and the collector junction is reverse biased which is known as forward active mode of operation. Forward biasing of emitter junction reduces the width of depletion layer at emitter junction and reverse biasing of collector junction results in increase of the width of depletion layer at the collector junction. It results in narrowing of base region and most of majority carriers injected from emitter to base region are able to reach at the collector junction with very few recombining in the base region of the transistor.

The BJT operates in inverse mode when collector junction forward biased and emitter junction reversed biased. A BJT is never operated in inverse mode because in inverse mode the emitter is reverse biased and heat dissipated from emitter junction is not enough due to its small size. This ultimately leads to thermal damage of the BJT which is also called thermal breakdown/thermal runway/secondary breakdown.

When BJT is used as a switch, it behaves like a closed switch, when both emitter and collector junctions are forward biased and it behaves like an open switch when both emitter and collector junctions are reversed biased. BJT can be used as a switch up to 10 kHz.

3.2 Operation of BJT as an Amplifier

The BJT can be operated as an amplifier by forward biasing the emitter junction and reverse biasing the collector junction. The operation of BJT as an amplifier can be simplified by taking an example of pnp transistor because of direction of current is same as direction of hole movement. When emitter junction of pnp type BJT is forward biased, the holes are injected from emitter to base region. As the width of base region of BJT is kept less than the diffusion length of minority carriers so most of the holes injected from emitter are passed to collector junction with very few recombining with electrons in the base region. Normally 98 to 99% of the carriers coming from emitter side are passed to collector side and only 1 – 2% recombine at the base region as shown in Fig.3. These holes injected from emitter to base and finally collected at collector junction with few recombining in base reason form i_{pE} component of emitter current, i_{pC1} component of collector current and $(i_{pE} - i_{pC1})$ component of base current. Here, $(i_{pE} - i_{pC1})$ is called recombination component of base current.

Under forward biased condition of base-emitter junction the electrons are injected from base region to emitter region which form i_{nE} component of emitter current. When collector junction of BJT is reverse biased there is jumping thermally generated holes from base to collector and thermally generated electrons from collector to base. These jumping of these thermally generated electrons and holes across the collector junction the reverse saturation current i_{CO} of collector junction flowing

from base to collector junction.

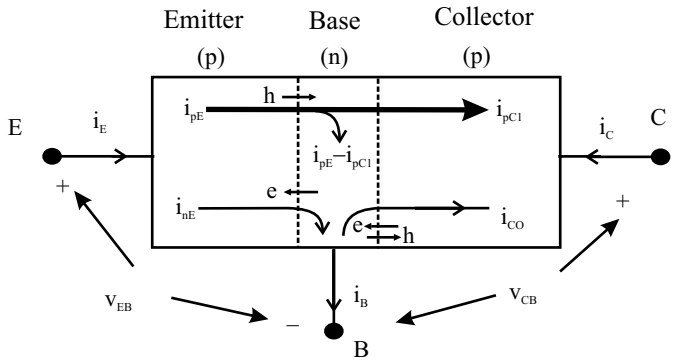


Fig. 3 Electrons and hole flow across the junctions of BJT

The emitter, base and collector current under forward biased mode of BJT can be given as under,

$$i_E = i_{nE} + i_{pE} \quad (1)$$

$$i_C = i_{pC1} + i_{CO} \quad (2)$$

$$i_B = i_{nE} + (i_{pE} - i_{pC1}) - i_{CO} \quad (3)$$

The reverse saturation current in base-collector junction is negligible. So, if this component of current is neglected then the collector and base currents become as under,

$$i_C = i_{pC1} \quad (4)$$

$$i_B = i_{nE} + (i_{pE} - i_{pC1}) \quad (5)$$

Base Transport Factor (B):

The component of collector current (i_{pC1}) due to holes is proportional to the holes component of emtter current. So, collector current (i_{pC1}) can be given in terms of i_{pE} as under,

$$i_{pC1} = Bi_{pE} \quad (6)$$

The proportionality factor B is fraction of holes reaching at collector which were injected from emitter. The factor B is called *base transport factor.*

The reverse saturation current in base-collector junction is neglected then,

$$i_C = Bi_{pE} \quad (7)$$

Emitter Injection Efficiency (γ):

The ratio of hole current (i.e. majority carrier) to the total emitter current is called emitter injection efficiency.

$$\therefore \quad \gamma = \frac{i_{pE}}{i_{pE}+i_{nE}} = \frac{i_{pE}}{i_E} \quad (8)$$

The emitter injection efficiency can also be given by,

$$\gamma \approx \frac{1}{1+\frac{p_{Eo}}{n_{Bo}}} = \frac{1}{1+\frac{n_i^2/N_E}{n_i^2/N_B}} = \frac{1}{1+\frac{N_B}{N_E}} \quad (8a)$$

Note : Ideally B and γ should be unity.

Current Transfer Ratio or Common Base Current gain (α):

Common base current gain or current transfer ratio of BJT is defined as ratio of collector current to the emitter current. So, the relation between collector current and emitter current can be given by,

$$\alpha = \frac{i_C}{i_E} = \frac{Bi_{pE}}{i_E} = B\gamma \quad (9)$$

The current gain 'α' depends upon width of the base region. As collector current is fraction of emitter current so the common base current gain α of BJT is always less than unity. It is of order of 0.99 to 0.995.

Base Current in Terms of Base Transport Factor :

The base current of BJT has three components. One due to electrons injected from base to emitter, second due to recombination of minority carriers i.e. holes injected from emitter and recombining in base region and third due to reverse saturation current through reverse biased base-collector junction. If 3rd component of base current is neglected then the base current can be obtained from equations (5) and (6) as under,

$$i_B = i_{nE} + (1-B)i_{pE} \quad (10)$$

Note : If B is fractions of holes reaching from emitter to collector junction then the fraction of holes recombining in base region is 1 – B.

Common Emitter Current gain or base to collector current amplification factor (β) :

The common emitter current gain is defined as the ratio of collector current to the base current.

$$\beta = \frac{}{i_B} = \frac{Bi_{pE}}{i_{nE}+(1-B)i_{pE}} = \frac{B[i_{pE}/(i_{pE}+i_{nE})]}{1-B[i_{pE}/(i_{pE}+i_{nE})]}$$

$$\Rightarrow \quad \beta = \frac{B\gamma}{1-B\gamma} = \frac{\alpha}{1-\alpha} \quad (11)$$

Since α of BJT is very small so β of the BJT is very large.

If τ_p is average life time of holes in base and τ_t is transition time of holes in base region then the common emitter current gain is also given by,

$$\beta = \frac{\tau_p}{\tau_t} \quad (12)$$

Example 1

The DC current gain (β) of a BJT is 50. Assuming that the emitter injection efficiency is 0.995, the base transport factor is

(a) 0.980 (b) 0.985

(c) 0.990 (d) 0.995

GATE(EC/2007/2M)

Solution: Ans.(b)

The emitter injection efficiency of BJT is ratio of majority carrier current component of emitter reaching to the collector to the total emitter current. For a pnp transistor the emitter injection efficiency is given by,

$$\gamma = \frac{I_{pE}}{I_{nE}+I_{pE}} = \frac{I_{pE}}{I_E}$$

$$\Rightarrow \quad I_E = \frac{I_{pE}}{\gamma} \qquad ...(i)$$

The base transport factor is the ratio of collector current to the majority carrier component of emitter current reaching at collector. For a pnp transistor the base transport factor is given by,

$$B = \frac{I_C}{I_{pE}}$$

$$\Rightarrow \quad I_C = BI_{pE} \qquad ...(ii)$$

Common base gain of BJT is given by,

$$\alpha = \frac{I_C}{I_E} \qquad ..(iii)$$

From (i) , (ii) and (iii), we have,

$$\alpha = B\gamma \qquad ..(iv)$$

Also,
$$\alpha = \frac{\beta}{1+\beta} \qquad ...(v)$$

β is common emitter current gain of BJT.

From (iv) and (v) , we have,

$$\frac{\beta}{1+\beta} = B\gamma$$

Given $\beta = 50$ and $\gamma = 0.995$

$$\Rightarrow \quad \frac{50}{1+50} = B\times 0.995$$

$$\Rightarrow \quad B = 0.985$$

3.3 Modes of Operation of BJT and Minority Carrier Distribution

A bipolar junction transistor can be operated in for different modes of operation known as forward or normal active region, inverse active region, cutoff region and saturation region. The regions of operation of BJT and corresponding distribution of minority carriers in emitter, base and collector regions are discussed as under,

I. Forward or Normal Active Mode

A BJT operates in forward active mode when B-E junction is forward biased and B-C junction is reverse biased.

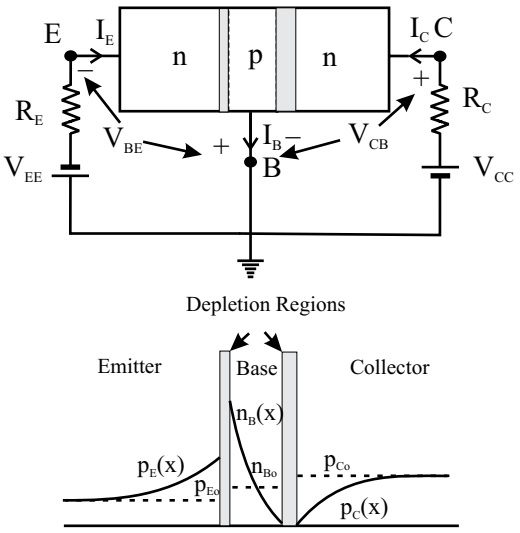


Fig.4 Minority carrier distribution in forward active mode

When a BJT is biased in forward active mode the electrons from emitter are injected into the base region and holes from the base region are injected in the emitter region. So, the concentration of minority carriers in emitter and base is maximum at the edges of depletion layer of B-E junction. The collector junction is reverse biased so the concentration of minority carriers is zero at edges of depletion layer of B-C junction as shown in the Fig.4

II. Inverse Active Mode

A BJT operates in inverse active mode when B-E junction is reverse biased and B-C junction is forward biased.

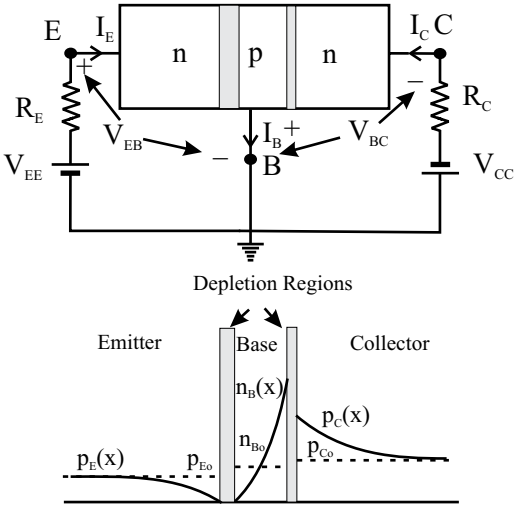


Fig.5 Minority carrier distribution in reverse active mode

When the BJT is biased in inverse mode the electrons from collector are injected into the base region and holes from the base region are injected in the collector region. So, the concentration of

minority carriers in collector and base is maximum at the edges of depletion layer of B-C junction. The emitter junction is reverse biased so the concentration of minority carriers is zero at edges of depletion layer of B-E junction as shown in the Fig.5.

III. Cutoff Mode

A BJT operates in cutoff mode both B-E junction and B-C junction are reverse biased. When both emitter and collector junctions are reverse biased the concentration of minority carriers become zero at the edges of depletion layers of both junction as shown in Fig.6

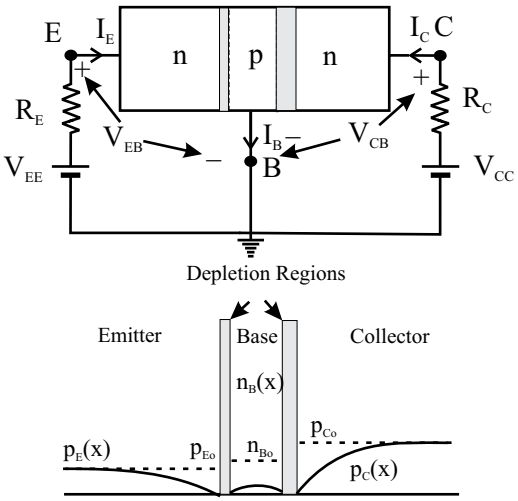


Fig.6 Minority carrier distribution in forward active mode

IV. Saturation Mode

A BJT operates in saturation when both B-E and B-C junctions are forward biased. When both junctions are forward biased the concentration of minority carriers is maximum at the edges of depletion layers of the junctions. The distribution of minority carriers in emitter, base and collector layers under saturation mode is as shown in the Fig.7.

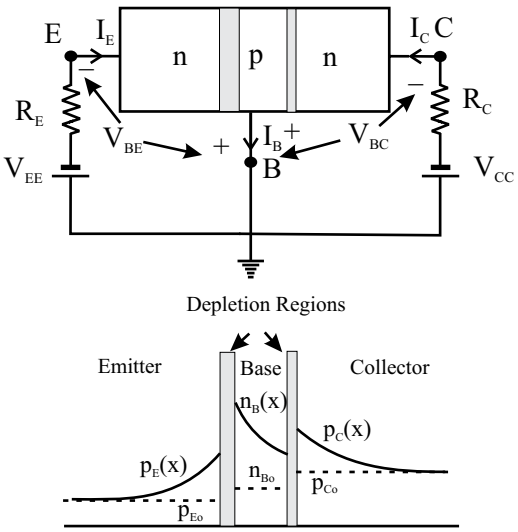
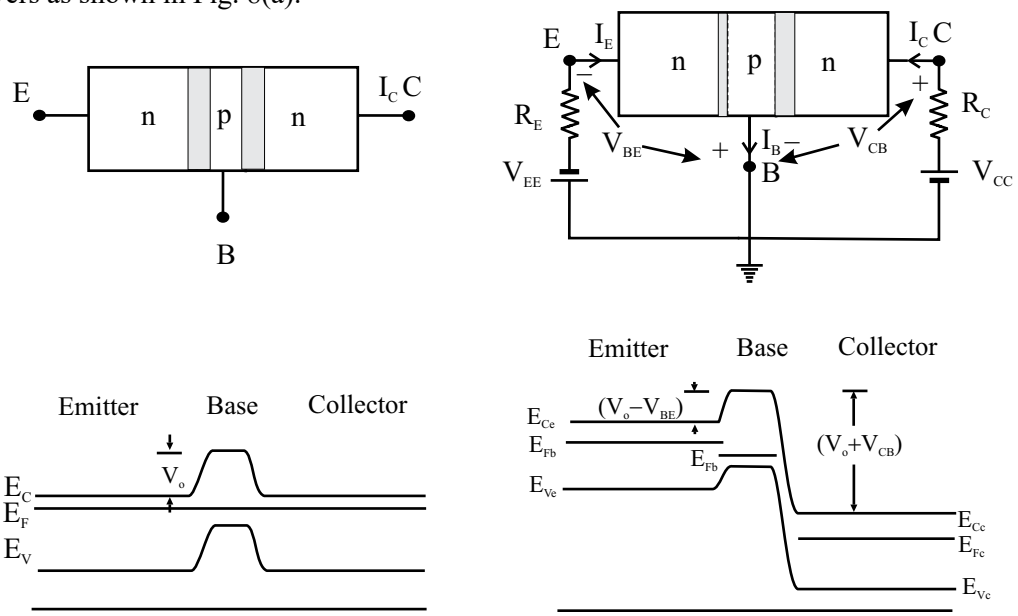


Fig.7 Minority carrier distribution in reverse active mode

3.4 Energy Band Diagram of BJT under Zero Bias and Active Mode

The Fermi level in open circuited condition is at same level across all the emitter , base and collector layers as shown in Fig. 8(a).



(a) Open Circuited (b) Active mode

Fig. 8 Energy band diagram of BJT under zero bias and active mode

In forward active mode E-B junction is forward based the Fermi level in emitter shifts upward and in Base region shifts down ward. The C-B junction is reverse biased resulting in shift of Fermi level in collector downward. This results in reduction in potential barrier at emitter junction from V_o to $V_o - V_{BE}$ and increase in potential barrier at collector junction from V_o to $V_o + V_{CB}$ as shown in Fig. 8(b) The width of depletion at emitter junction becomes narrower and width of depletion layer at collector junctions gets widened. As emitter junction is forward biased the electrons from n-layer of emitter are injected to base layer of base region. These electrons are minority carriers in base region and diffuse towards the collector junction. As width of the base region is kept less than the diffusion length of electrons so the electrons reaching at the collector junction falls down the potential hill towards the collector layer with very few recombining in the base region. These electrons which falls down the potential hill at collector junction form the major part of collector current in the BJT which is responsible for amplifier action of BJT. The number of electrons recombining in the base region of BJT depends on base width as well as doping level of base region.

3.5 Simplified Current Expressions of BJT

The current and voltage relations in BJT under forward active mode can be derived by using concentration gradient of minority carrier in base region. The electrons injected from emitter region are diffused to collector junction through base region due to concentration gradient across the base. Ideally the concentration gradient in base region is linear across the width of base which implies

no recombination as shown in Fig. 9. The electrons which diffuse across the base are swept into collector region by electric field in depletion region of collector junction.

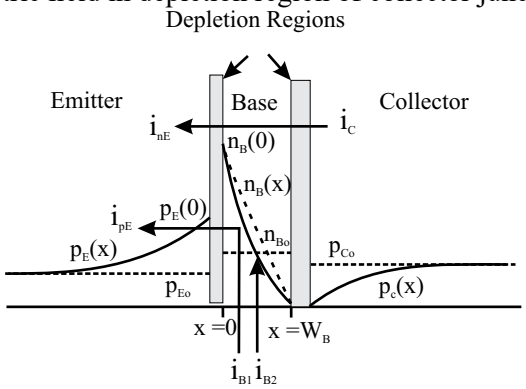


Fig.9 Minority carrier distribution and current components in forward active mode

Collector Current:

Ideally, the approximately same as collector current is same as the emitter current due to electrons at edge of depletion layer of emitter junction at x = 0. So, the collector current density can be given by,

$$i_C = i_{nE} = qA_E D_n \frac{dn}{dx} \tag{13}$$

where D_n is diffusion constant of electrons in base region and dn/dx is concentration gradient in the base region and A_E is cross-section area of B-E junction. If no recombination occurs in the base region then concentration of minority carriers varies linearly in the base region then,

$$\frac{dn}{dx} = \frac{n_B(0) - 0}{0 - W_B} = -\frac{n_B(0)}{W_B} \tag{14}$$

Where $n_B(0)$ is concentration of electrons at the edge of depletion layer at collector junction in base and W_B is neutral or effective width of base region. W_B is measured from edge of depletion layer on emitter side to edge of depletion layer on collector side. There is one more term known as metallurgical width of base which is junction to junction width of base region. The metallurgical width will be denoted by L_B in this chapter.

$$\Rightarrow \quad i_C = -qA_E D_n \frac{n_B(0)}{W_B} \tag{15}$$

The concentration of minority carriers at the edge (i.e. at x = 0) of depletion layer of a B-E junction can be given by,

$$n_B(0) = n_{Bo} e^{\frac{V_{BE}}{V_T}} \tag{16}$$

Where n_{Bo} is concentration of electrons in base region at thermal equilibrium, V_{BE} is forward biasing voltage of B-E junction and V_T (= kT/q or T/11600 V) is thermal voltage. The thermal voltage 25 mV at room temperature. The above equation has already been derived in pn junction diodes.

The concentration of electrons at thermal equilibrium is given by,

$$n_{Bo} = \frac{n_i^2}{N_B} \tag{16a}$$

Where n_i is intrinsic concentration and N_B is doping concentration of base region.
The excess minority carrier cancentration at the edge of deplation layer of B-E junction at x = 0 can be given by,

$$\delta n_B(0) = n_B(0) - n_{Bo} = n_{Bo} e^{\frac{V_{BE}}{V_T}} - n_{Bo} = n_{Bo}\left(e^{\frac{V_{BE}}{V_T}} - 1\right) \tag{16b}$$

Thus the magnitude of collector current becomes,

$$\Rightarrow \quad \boxed{i_C = \frac{qA_E D_n n_{Bo}}{W_B} e^{\frac{V_{BE}}{V_T}}} \tag{17}$$

or
$$i_C = I_S e^{\frac{V_{BE}}{V_T}} \tag{18}$$

where,
$$I_S = \frac{qA_E D_n n_{Bo}}{W_B} \tag{19}$$

It is observed from equation (17) that the collector current is controlled by the forward biasing base-emitter voltage (V_{BE}). It is not function of voltage across the collector-base junction (V_{CB}).

Emitter Current:

The emitter current of BJT has two components i_{nE} and i_{pE}. The component i_{nE} of emitter current is due to injection of electrons from emitter to base region. This component is same as i_C given by the equation (17). The second component i_{pE} is due to holes injected from base region to emitter region. The second component of emitter current can be obtained current equation of a forward biased pn junction which is given by,

$$i_{pE} = I_{S2} e^{\frac{V_{BE}}{V_T}} \tag{20}$$

where I_{S2} can be given by,

$$I_{S2} = \frac{qA_E D_p p_{Eo}}{L_p} \tag{21}$$

Where, D_p diffusion constant of holes in emitter and L_p is diffusion length of holes in emitter region, p_{Eo} is concentration holes in emitter region at thermal equilibrium. Therefore, total emitter current can be given by,

$$i_E = i_{nE} + i_{pE} = i_C + i_{pE} = I_S e^{\frac{V_{BE}}{V_T}} + I_{S2} e^{\frac{V_{BE}}{V_T}} \tag{22}$$

$$\Rightarrow \quad i_E = I_{SE} e^{\frac{V_{BE}}{V_T}} \tag{23}$$

where, $$I_{SE} = I_S + I_{S2} \tag{24}$$

Base Current:

The component of emitter current due holes injected from base to emitter also forms one component of the base current. Thus, base current is also function of the factor $e^{\frac{V_{BE}}{V_T}}$. The second component of base current is due to recombination of minority carriers in the base region.

Common Base Gain:

The common base current gain of BJT of the transistor is given by,

$$\alpha = \frac{i_C}{i_E} = \frac{I_S e^{\frac{V_{BE}}{V_T}}}{I_S e^{\frac{V_{BE}}{V_T}} + I_{S2} e^{\frac{V_{BE}}{V_T}}} = \frac{I_S}{I_S + I_{S2}} = \frac{1}{1 + I_{S2}/I_S}$$

$$\Rightarrow \quad \alpha = \frac{1}{1 + \frac{W_B D_p p_{Eo}}{L_p D_n n_{Bo}}} = \frac{1}{1 + \frac{W_B D_p (n_i^2/N_E)}{L_p D_n (n_i^2/N_B)}} = \frac{1}{1 + \frac{W_B D_p N_B}{L_p D_n N_E}} \tag{25}$$

Example 2

The neutral base width of a bipolar transistor, biased in the active region, is 0.5 μm. The maximum electron concentration and the diffusion constant in the base are $10^{14}/cm^3$ and $D_n = 25\ cm^2/sec$ respectively. Assuming negligible recombination in the base, the collector current density is (the electron charge is 1.6×10^{-19} coulomb)

(a) $800\ A/cm^2$ (b) $8\ A/cm^2$

(c) $200\ A/cm^2$ (d) $2\ A/cm^2$

GATE(EC/2004/2M)

Solution: Ans.(b)

Ideally, the collector current density is same as the emitter current density due to electrons at edge of depletion layer of emitter junction at x = 0. So, the collector current density can be given by,

$$J_C = J_{nE} = qD_n \frac{dn}{dx}$$

where D_n is diffusion constant of electrons in base and dn/dx is concentration gradient in the base region. If no recombination occurs in base region then the concentration varies linearly in the base region then,

$$\frac{dn}{dx} = \frac{n_B(0) - 0}{0 - W_B} = -\frac{n_B(0)}{W_B}$$

Where $n_B(0)$ is concentration of electrons at the edge of depletion layer at collector junction in base

and W_B is neutral width of base region.

$$\Rightarrow \quad J_C = -qD_n \frac{n_B(0)}{W_B}$$

Given, $n_B(0) = 10^{14}/cm^3$ and $D_n = 25\ cm^2/sec$,

Base width, $W_B = 0.5\ \mu m = = 0.5\times10^{-4}$ cm. Taking only magnitude the collector current density becomes as under,

$$J_C = 1.6 \times 10^{-19} \times 25 \times \frac{10^{14}}{0.5\times10^{-4}}\ A/cm^2 = 8\ A/cm^2$$

Example 3

Consider two BJTs biased at the same collector current with area $A_1 = 0.2\ \mu m \times 0.2\ \mu m$ and $A_2 = 300\ \mu m \times 300\ \mu m$. Assuming that all other device parameters are identical, kT/q = 26 mV, the intrinsic carrier concentration is $1 \times 10^{10}\ cm^{-3}$, and $q = 1.6 \times 10^{-19}$ C, the difference between the base-emitter voltage (in mV) of the two BJTs (i.e., $V_{BE1} - V_{BE2}$) is_____

GATE(EC-IV/2014/2M)

Solution:Ans (378 to 381)

Thus the magnitude of collector current becomes,

$$i_C = \frac{qA_E D_n n_{Bo}}{W_B} e^{\frac{V_{BE}}{V_T}}$$

Where, A_E is cross-section area of emitter junction, D_n is diffusion constant of electrons in base, n_{Bo} is concentration of electrons in base at thermal equilibrium and W_B is neutral or effective width of base.

If D_n, n_{Bo}, W_B are same for both transistors then,

$$i_C \propto A_E e^{\frac{V_{BE}}{V_T}}$$

$$\Rightarrow \quad \frac{i_{C1}}{i_{C2}} = \frac{A_{E1} e^{\frac{V_{BE1}}{V_T}}}{A_{E2} e^{\frac{V_{BE2}}{V_T}}}$$

$$\Rightarrow \quad \frac{i_{C1}}{i_{C2}} = \frac{A_{E1}}{A_{E2}} e^{\frac{(V_{BE1}-V_{BE2})}{V_T}}$$

Given, $i_{C2} = i_{C1}$, $V_T = kT/q = 26$ mV,

$A_{E2} = A_2 = 300\ \mu m \times 300\ \mu m$

$A_{E1} = A_1 = 0.2\ \mu m \times 0.2\ \mu m$

$$\Rightarrow \quad 1 = \frac{0.2\times0.2}{300\times300} e^{\frac{(V_{BE1}-V_{BE2})}{26\times10^{-3}}}$$

$$\Rightarrow \quad V_{BE1} - V_{BE2} = 380.28\ mV$$

Example 4

An npn BJT having reverse saturation current $I_s = 10^{-15}$ A is biased in the forward active region with $V_{BE} = 700$ mV. The thermal voltage (V_T) is 25 mV and the current gain (β) may vary from 50 to 150 due to manufacturing variations. The maximum emitter current (in μA) is .....

GATE(EC-III/2015/2M)

Solution: (1465 to 1485)

The collector current of BJT is given by,

$$i_c = I_s e^{\frac{V_{BE}}{V_T}}$$

Given, $V_{BE} = 700$ mV, $V_T = 25$ mV, $I_s = 10^{-15}$ A

$$\therefore \quad i_c = 10^{-15} \times e^{\frac{700\times10^{-3}}{25\times10^{-3}}} = 1.446\,\text{mA}$$

Given $\beta = 50$ to 150

Corresponding value of α, $\alpha = \dfrac{\beta}{1+\beta}$

$$\Rightarrow \quad \alpha = \frac{50}{1+50} \text{ to } \frac{150}{1+150} = 0.980 \text{ to } 0.993$$

The emitter current in terms of collector current is given by,

$$i_E = \frac{i_c}{\alpha}$$

When $\alpha = 0.980$, $\quad i_E = \dfrac{1.446}{0.98}\text{mA} = 1475.77\,\mu\text{A}$

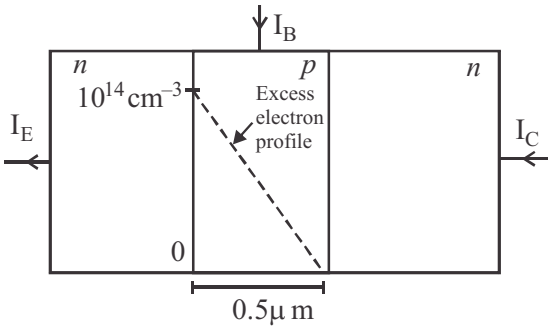
When $\alpha = 0.993$, $\quad i_E = \dfrac{1.446}{0.993}\text{mA} = 1456.19\,\mu\text{A}$

So, maximum emitter current is 1475.77 μA

Example 5

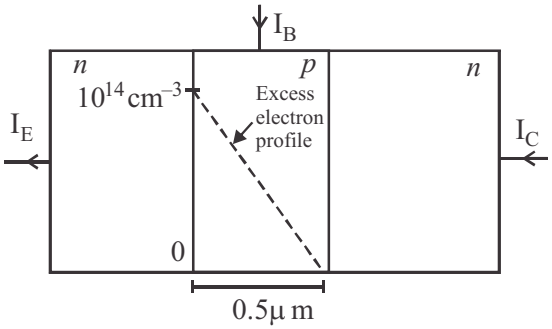
The injected excess electron concentration profile in the base region of an *npn* BJT, biased in the active region, is linear, as shown in the figure. If the area of the emitter-base junction is 0.001 cm^2, $\mu_n = 800$ $cm^2/(V\text{-}s)$ in the base region and depletion layer widths are negligible, then the collector current I_C (in mA) at room temperature is .....

(Given: thermal voltage $V_T = 26$ mV at room temperature, electronic charge $q = 1.6 \times 10^{-19}$ C)



GATE(EC-III/2016/2M)

Solution : Ans. (6.55 to 6.75)



Ideally, the collector current density is same as the emitter current density due to electrons at edge of depletion layer of emitter junction at x = 0. So, the collector current can be given by,

$$I_C = I_{nE} = qA_E D_n \frac{dn}{dx}$$

Where D_n is diffusion constant of electrons in base and dn/dx is concentration gradient in the base region, A_E is area of emitter junction. If no recombination occurs in base region then the concentration varies linearly in the base region then,

$$\frac{dn}{dx} = \frac{n_B(0) - 0}{0 - W_B} = -\frac{n_B(0)}{W_B}$$

Where $n_B(0)$ is concentration of electrons at the edge of depletion layer at collector junction in base and W_B is neutral width of base region.

$$\Rightarrow \quad I_C = -qA_E D_n \frac{n_B(0)}{W_B}$$

From the given figure, $n_B(0) = 10^{14}/cm^3$ and $W_B = 0.5\ \mu m = 0.5 \times 10^{-4}$ cm,
Also given $\mu_n = 800\ cm^2/(V\text{-}s)$, $q = 1.6 \times 10^{-19}$ C, $A_E = 0.001\ cm^2$ and thermal voltage, $V_T = 26$ mV.
As per Einstein relation, the Diffusion constant of electrons,

$$D_n = \mu_n V_T$$

$$\Rightarrow \quad D_n = 800 \times 26 \times 10^{-3}\ cm^2/sec = 20.8\ cm^2/sec$$

Taking only magnitude the collector current density becomes as under,

$$I_C = 1.6\times10^{-19}\times0.001\times20.8\times\frac{10^{14}}{0.5\times10^{-4}}\text{A}$$

$$\Rightarrow \quad I_C = 6.656\text{ mA}$$

3.6 Components of Current in BJT

The components of current in BJT amplifier working in forward active mode with emitter junction forward biased and collector junction reverse biased can be explained by taking a pnp transistor as shown in Fig. 10.

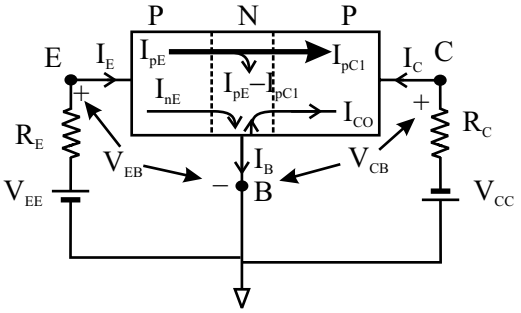


Fig. 10 BJT current components during foward active mode

Emitter Current (I_E):

The emitter current of transistor (I_E) consists of hole current (I_{pE}) due to holes injected from emitter to base region and electron current (I_{nE}) due to injected electrons from base to emitter region.

$$\therefore \quad I_E = I_{pE} + I_{nE} \tag{26}$$

Since emitter region is heavily doped as compared to the base region therefore, the hole current (I_{pE}) is very large compared to electron current (I_{nE}). Ideally, the emitter current is assumed to entirely due to holes (i.e. $I_E \approx I_{pE}$). This is desirable because I_{nE} does not contribute carriers which can reach to collector junction for amplifier operation.

Base Current (I_B):

As discussed in previous section that the base current of BJT has three components. One component is due to electrons injected from base to emitter (I_{nE}), second component is recombination current due to recombination of minority carriers i.e. holes injected from emitter and recombining in base region (i.e. $I_{pE} - I_{pC1}$) and third component is reverse saturation current due to jumping of thermally generated electrons and holes through reverse biased base-collector junction ($I_{CO} = I_{nCO} + I_{pCO}$). The 3rd component of base current is negligible. Thus the total base current can be given by,

$$I_B = I_{nE} + (I_{pE} - I_{pC1}) - I_{nCO} - I_{pCO} = I_{nE} + (I_{pE} - I_{pC1}) - I_{CO} \tag{27}$$

Where I_{pC1} is component of collector current due to holes reaching at collector junction which were injected from emitter region.

Collector Current (I_C):

The total collector current has two components. One component is due to holes reaching from emitter

to collector junction (I_{pC1}) and second component is due to reverse saturation current (I_{CO}) through reverse biased base-collector junction.

$$I_C = I_{pC1} + I_{CO} \quad (28)$$

$$I_{pC1} = \alpha I_{pE} \approx \alpha I_E \quad (29)$$

$$\boxed{I_C = \alpha I_E + I_{CO}} \quad (30)$$

where I_{CO} is reverse saturation current between collector and base.

The generalized exact expression of collector current can be writer as under,

$$\boxed{I_C = \alpha I_E + I_{CO}(1 - e^{V_{CB}/V_T})} \quad (31)$$

Relation between base current (I_B) and collector current (I_C):

The emitter current of BJT is equal to algebraic sum of collector and base currents.

$$\therefore \quad I_E = I_C + I_B \quad (32)$$

$$\Rightarrow \quad I_C = \alpha[I_C + I_B] + I_{CO}$$

$$\Rightarrow \quad I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CO} \quad (33)$$

$$\Rightarrow \quad \boxed{I_C = \beta I_B + (1+\beta) I_{CO}} \quad (34)$$

Relation between base current (I_B) and emitter current (I_E):

$$I_E = I_C + I_B \approx \beta I_B + I_B$$

$$I_E = (1 + \beta) I_B \quad (35)$$

Relation between common emitter current gain β and α:

$$I_E = I_C + I_B$$

$$\Rightarrow \quad \frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$$

$$\Rightarrow \quad \frac{1}{\alpha} = \frac{1}{\beta} + 1 \quad (36)$$

$$\Rightarrow \quad \boxed{\alpha = \frac{\beta}{1+\beta}} \quad (37)$$

$$\Rightarrow \quad \boxed{\beta = \frac{\alpha}{1-\alpha}} \quad (38)$$

Relation between leakage current between collector & base and between collector and emitter :

When base terminal is open circuited the base current is zero and there is leakage current between collector and emitter terminal. The leakage current between collector and emitter can be obtained by setting $I_B = 0$ in equation (34) as under,

$$I_{CEO} = (1 + \beta)I_{CO} \tag{39}$$

If emitter terminal is open circuited the current between collector and base is I_{CBO} . The current I_{CBO} can be obtained by setting $I_E = 0$ in equation (30) as under,

$$I_{CBO} = I_{CO} \tag{40}$$

From equations (39) and (40), we have,

$$\Rightarrow \quad \boxed{I_{CEO} = (1+\beta) I_{CBO}} \tag{41}$$

$$\Rightarrow \quad \boxed{I_{CEO} = \left(1 + \frac{\alpha}{1-\alpha}\right) I_{CBO} = \frac{1}{1-\alpha} I_{CBO}} \tag{42}$$

Note : *i. Practically $I_{CBO} > I_{CO}$ due to leakage current between collector and base terminals. But for all practical purposes $I_{CBO} = I_{CO}$.*

Common Collector Current Gain(γ') :

The common collector current gain is defined as the ratio of emitter current to the base current.

$$\gamma' = \frac{I_E}{I_B} \tag{43}$$

But $I_E = I_C + I_B$

$$\Rightarrow \quad \gamma' = \frac{I_C + I_B}{I_B} = 1 + \frac{I_C}{I_B}$$

$$\Rightarrow \quad \boxed{\gamma' = \beta + 1} \tag{44}$$

But $\beta = \frac{\alpha}{1-\alpha}$

$$\Rightarrow \quad \gamma' = \frac{\alpha}{1-\alpha} + 1 = \frac{1}{1-\alpha} \tag{45}$$

Example 6

For a BJT, the common-base current gain $\alpha = 0.98$ and the collector base junction reverse bias saturation current $I_{CO} = 0.6\ \mu A$. This BJT is connected in the common emitter mode and operated in the active region with a base drive current $I_B = 20\ \mu A$. The collector current I_C for this mode of

operation is

(a) 0.98 mA (b) 0.99 mA

(c) 1.0 mA (d) 1.01 mA

GATE(EC/2011/2M)

Solution : Ans.(d)

Collector current BJT in common emitter mode is given by,

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

or $$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CO}$$

Given, $\alpha = 0.98$, $I_B = 20\ \mu A$, $I_{CO} = 0.6\ \mu A$

$$\Rightarrow \quad I_C = \frac{0.98}{1-0.98} \times 20 + \frac{1}{1-0.98} \times 0.6\ \mu A = 1.01 mA$$

Example 7

An npn transistor connected as a common emitter switch has $I_{CBO} = 1\ \mu A$ and $h_{FE} = 100$. The OFF state current of this switch is of the order of

(a) 0.1 μA (b) 1.0 μA

(c) 10.0 μA (d) 100.0 μA

Solution : Ans (b)

Collector current of BJT is given by

$$I_C = \beta I_B + (1+\beta) I_{CBO} = \alpha I_E + I_{CBO}$$

The transistor in common emitter mode is off

When, $I_E = 0$

$\Rightarrow$ $I_C = I_{CBO}$

Given, $I_{CBO} = 1\ \mu A$

$\therefore$ $I_C = 1\ \mu A$ at off stable

Example 8

If $\alpha = 0.98$, $I_{CO} = 6\mu A$ and $I_B = 100\ \mu A$ for a transistor, then the value of I_C will be

(a) 2.3 mA (b) 3.1 mA

(c) 4.6 mA (d) 5.2 mA

IES(EE,02)

Solution : Ans (d)

Collector current of BJT amplifier is given by,

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

Where, $$\beta = \frac{\alpha}{1-\alpha}$$

Given, $\alpha = 0.98, I_{CO} = 6\ \mu A$

& $I_B = 100\ \mu A$

Then, $\beta = \frac{0.98}{1-0.98} = 49$

And $I_C = 49 \times 100 + (49 + 1) \times 6\ \mu A = 5.2\ \mu A$

Example 9

If $\alpha = 0.995$, $I_E = 1$ mA $I_{CO} = 0.5\ \mu A$, then I_{CEO} will be

(a) 100μA (b) 25 μA

(c) 10.1 mA (d) 10.5 mA

IES(EE,97)

Solution : Ans (a)

The collector current of BJT amplifier is given by,

$$I_C = \beta I_B + (1 + \beta) I_{CO}$$

Where, $\beta = \frac{\alpha}{1-\alpha}$

When, $I_B = 0$

$\Rightarrow$ $I_C = I_{CEO}$

$\Rightarrow$ $I_{CEO} = (1 + \beta) I_{CO}$

$\Rightarrow$ $I_{CEO} = \left(1 + \frac{\alpha}{1-\alpha}\right) I_{CO} = \frac{1}{1-\alpha} I_{CO}$

Given, $\alpha = 0.995$, $I_{CO} = 0.5\ \mu A$

$\Rightarrow$ $I_{CEO} = \frac{0.5}{1-0.995} = 100 \mu A$

Example 10

If the α value of a transistor changes 0·5% from its nominal value of 0·9, the percentage change in β will be

(a) 0% (b) 2·5%

(c) 5% (d) 7·5%

IES (E&T, 13)

Solution: Ans (c)

Given, $\alpha = 0{\cdot}9$ and $\Delta\alpha = 0{\cdot}5\%$ or 0.005

The current transfer ratio of BJT in CE mode,

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.9}{1-0.9} = 9$$

The value of α after 0.5% change, $\alpha' = 0.9 + 0.005 \times 0.9 = 0.9045$

New value of β, $$\beta' = \frac{\alpha'}{1-\alpha'} = \frac{0.9045}{1-0.9045} = 0.48$$

Percentage change in β, $$\Delta\beta = \frac{\beta'-\beta}{\beta} \times 100 = \frac{0.48-0.9}{0.9} \times 100 = -1.7\%$$

So, approximate change in β is 5% for change of 0.5% in α.

3.7 Configurations of BJT

The circuits of BJT can have three different configurations depending on which terminal is taken as common between input and output terminals. When base is taken as common the configuration is called common base (CB) configuration, when emitter is taken as common then configuration is called common emitter (CE) configuration and when collector is taken as common then configuration is called common collector (CC) configuration.

3.7.1 Common Base (CB) Configuration

The common base configuration has emitter terminal as input, the collector terminal as output and base terminal as common between input and output terminal as shown in the Fig.11.

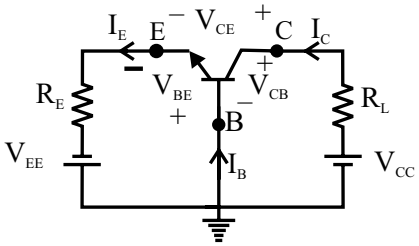


Fig. 11 Common base configuration of npn transistor

The direction of current I_E, I_B and I_C as shown in the circuit are positive for an npn transistor. The polarity of voltages V_{CB} and V_{BE} shown in the circuit are also positive for an npn transistor.

Input/static/emitter characteristics of common base configuration:

The input characteristics of CB configuration gives the relation between emitter junction voltage and emitter current for a particular voltage across the collector junction.

Input characteristic of CB is define by,

$$V_{BE} = f(V_{CB}, I_E) \quad (46)$$

Thus the input characteristics of common base configuration characteristics are same as the characteristics of a forward biased pn junction as shown in the Fig. 12.

The input characteristics exhibit a cut-in voltage (V_γ) of emitter junction. The cut-in voltage is 0.1 V for Ge and 0.5 V for Si. The emitter current I_E increases with increase in V_{CB} for constant V_{BE} due to an effect known as early effect.

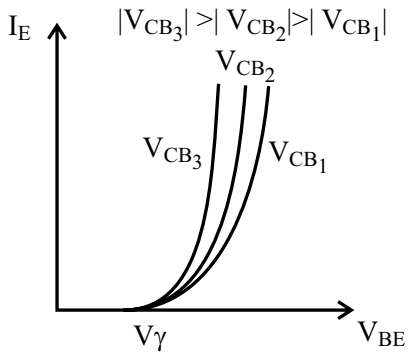


Fig. 12 Input characteristics of common base configuration of npn transistor

Output characteristics of CB configuration :

Output characteristic of CB configuration gives variation of collector current as a function of V_{CB} and I_E.

$$I_C = f(V_{CB}, I_E) \quad (47)$$

The output characteristics of npn transistor are shown in Fig. 13. It is observed from the Fig. 13 that the output characteristics of CB configuration has three regions of operation called active, saturation and cut-off.

1. **Active region:** In active region emitter junction is forward biased and collector junction is reverse biased. In this region of operation output collector current (I_C) increases linearly with increase in input emitter current(I_E). Therefore, transistor behaves like a linear amplifier in active region. The collector current as a function of emitter current in active region is given by

$$I_C = \alpha I_E + I_{CO} \quad (48)$$

When the input current becomes zero the collector current is equal I_{CO} which is also denoted by I_{CBO}. The current I_{CO} is called leakage current of BJT which is similar to reverse saturation current of a pn junction. The collector current in active region is almost independent of V_{CB} . However, the collector increases slightly with V_{CB} due to early effect.

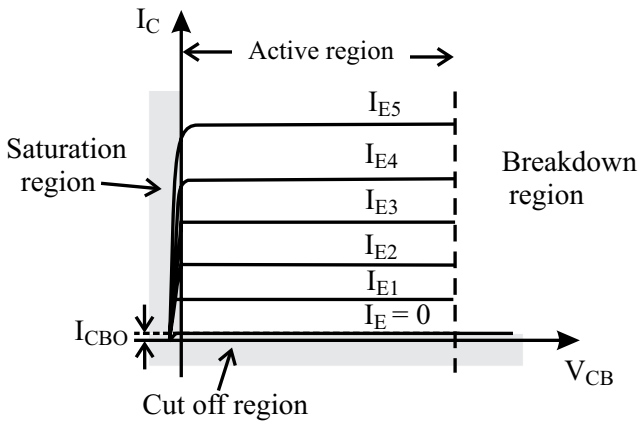


Fig. 13 Output characteristics of common base configuration of npn transistor

2. **Saturation region:** In this region both collector and emitter junctions are forward biased. The region to left of $V_{CB} = 0$ and above $I_E = 0$ is saturation region in output characteristics. The BJT behaves like a closed switch in saturation region. There is exponential change in collector current with small change in V_{CB} in saturation region.
3. **Cut off region :** In this region both emitter and collector junctions are reverse biased. The collector current is negligible *i.e.* reverse saturation current I_{CO}. The region below $I_E = 0$ in output characteristics is cutoff region. The transistor behaves like an open switch in cut off region.
4. **Break down region :** When the reverse biasing voltage of collector junction exceeds the breakdown voltage of the junction, their is avalanche multiplication resulting into sudden increase of collector current. A transistor is never operated in break down region because it may lead to thermal breakdown of the transistor.
5. **Inverse active mode :** In this mode of operation emitter junction is reversed biased and collector junction in forward biased. In inverse operation a transistor cannot be used as an amplifier because the heat dissipation at reverse biased emitter junction may not be sufficient due to its small size and ultimately it will lead to thermal breakdown of emitter junction.

Early Effect or Base Width Modulation:

When the reverse biasing voltage across the collector junction is increased the width of depletion layer at collector junction increases and hence metallurgical width of the base region reduces from L_B to neutral width W_B as shown in Fig.14. The minority carrier are able to cross the base region little early due to reduced width of base region caused by increased collector-base junction voltage (V_{CB}). This modulation of base width by collector voltage is called early effect.

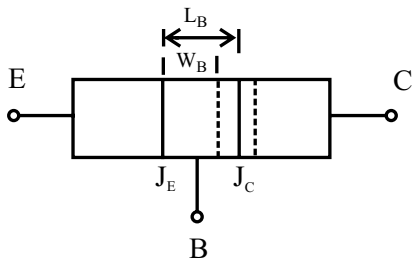


Fig. 14 Base width modulation due to early effect

Consequences of Early Effect:

i) As the effective width of base reduces the chances of recombination of injected minority carriers in the base region reduces. Therefore, the current gain 'α' increases.
ii) The concentration gradient of minority carriers in base region is increased due to increased depletion layer width at collector junction and reduced effective base width. Since component of emitter current due to injected minority carriers in base region is proportional to the concentration gradient of minority carriers in base region so the emitter current is increased. Thus, the emitter current increases with increase in collector-base junction voltage (V_{CB}).
iii) As the collector current I_C ($= \alpha I_E$) is directly proportional to α and I_E so the collector current is also increases with increase in V_{CB} due to the early effect.
iv) The common base gain $\beta = \alpha/(1-\alpha)$ also increases with increase in a due to early effect.
iii) At high voltage across the collector junction whole base region may be covered by the depletion

layer, resulting into a condition called punch through or reach through. Under this condition transistor no more behaves like an amplifier. If voltage V_{CB} is increased beyond punch through then the effective voltage at base-emitter junction is also reduced due to fall in junction barrier.

iv) The base current reduces because of reduction in recombination of base region.

Current Gains of Common Emitter Configuration :

1. dc current gain:

The dc current gain of CB configuration is defined as ratio of I_C to I_E.

$$\alpha_{dc} = \frac{I_C}{I_E} \tag{49}$$

2. Small signal current gain

The small signal gain of CB configuration is defined as ratio of differential change in collector current to differential change in emitter current with fixed collector to base voltage V_{CB}.

$$\alpha_{ac} = \left.\frac{\partial i_c}{\partial i_e}\right|_{V_{CB} = \text{constant}} \tag{50}$$

3. Large signal current gain

The large signal gain of CB configuration is obtained from the relation collector current with emitter current as under,

$$I_C = \alpha I_E + I_{CO} \tag{51}$$

$$\alpha = \frac{I_C - I_{CO}}{I_E} = \text{Large signal current gain} \tag{52}$$

If I_{CO} is neglected then $\alpha = \alpha_{dc}$

Important parameters of CB configuration:

i) It has low input impedance (≈100 Ω) and very high output impedance (≈500 kΩ).

ii) Current gain is less than unity (order of 0.9)

iii) Voltage gain is high (order of 150)

iv) Input and output signals are in phase with each other.

v) Leakage current is small.

Note : *i. For switching application BJT is operated in saturation and cut off region and for amplifier applications BJT is operated in active region.*

ii. Common base configuration is mostly used at high frequencies in radio frequency (RF) range.

3.7.2 Common Emitter (CE) Configuration

The common emitter configuration of BJT has base terminal as input, the collector terminal as output and emitter terminal as common between input and output terminals as shown in the Fig.15.

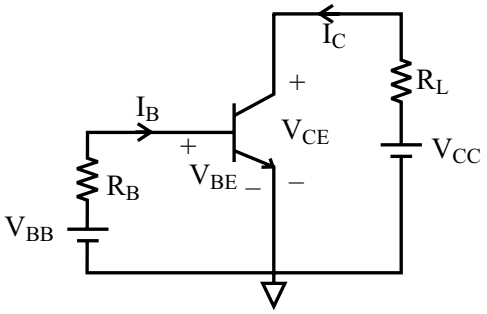


Fig. 15 Common base configuration of npn transistor

Input characteristics of common emitter configuration:

The input characteristics of CE configuration gives the variation of voltage V_{BE} as a function of V_{CE} and I_B as shown in Fig. 16. Input characteristics of CE configuration are define by,

$$V_{BE} = f(V_{CE}, I_B) \quad (53)$$

It observed from the input characteristics that the increase in voltage V_{CE} results in increase in depletion layer width and reduction in effective base width so the chances of recombination of minority carriers in the base region are reduced hence recombination component of base current is reduced. Therefore, the base current decreases with increase in V_{CE} for fixed value of voltage V_{BE}.

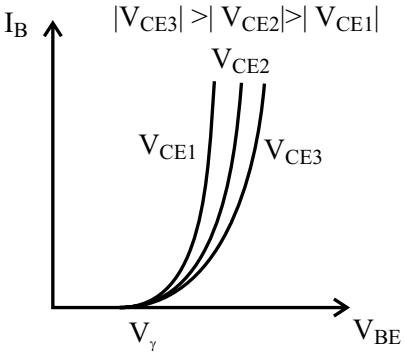


Fig. 16 Input characteristics of common emitter configuration of npn transistor

Note : V_γ is 0.1 V to 0.2 V for Ge and 0.5 V to 0.6 V for Si.

Output characteristics of CE configuration :

Output characteristic of CE configuration gives variation of collector current as a function of V_{CE} and I_B.

$$I_C = f(V_{CE,} I_B) \quad (54)$$

The output characteristics of npn transistor are shown in Fig. 17. It is observed from the Fig. 17 that the output characteristics of CE configuration has three regions of operation called active, saturation and cut-off.

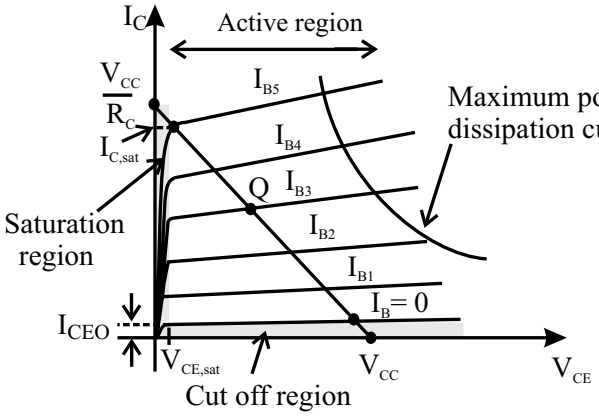


Fig. 17 Output characteristics of common emitter configuration of npn transistor

From the collector circuit, $V_{CE} = V_{CC} - I_C R_C$

$$\Rightarrow \quad I_C = \frac{-1}{R_C} V_{CE} + \frac{1}{R_C} V_{CC} \tag{55}$$

Above equation represent dc load line which is drawn in output characteristics of CE configuration in Fig. 17. The slope of dc load line is $\frac{-1}{R_C}$. The intersection of load line with output characteristics of BJT is known as Q-point or operating point.

Regions of operation of CE configuration:

1. **Active region:** The transistor operates in active region when emitter junction is forward biased and collector junction is reverse biased. The transistor behaves like a linear amplifier in active region. The collector current varies almost linearly with the base current. The collector current in terms of base current in active region is given by,

$$I_C = \beta I_B + (1 + \beta) I_{CO} = \frac{\alpha}{1 - \alpha} I_B + \frac{1}{1 - \alpha} I_{CO} \tag{56}$$

Where β is common emitter current gain and I_{CO} is leakage current or reverse saturation current between base and collector.

It is observed from the output characteristics that the collector current is not independent of V_{CB} unlike common base configuration because the current gain α increases with increase in voltage V_{CB} due to early effect and small increase in α results in large increase in β [i.e. $\alpha/(1-\alpha)$] for example change in a from 0.98 to 0.99 results in change in b from 49 [i.e. 0.98/(1-0.98)] to 99 [i.e. 0.99/(1-0.99)] and hence the collector current increases with increases in voltage V_{CB} in CE configuration in active region of operation.

Note : When collector terminal of BJT is shorted with the base terminal the BJT works in active region and its characteristics are similar to a pn junction diode.

2. **Cut-off region**

At cutoff the collector current should be equal to I_{CO} and emitter current is zero. This condition

is not met when input base current is zero which illustrated as under,
The collector current of BJT is given by,

$$I_C = \beta I_B + (1 + \beta) I_{CO} \quad (57)$$

when, $$I_B = 0, I_C = I_{CEO} = (1+\beta) I_{CO} \quad (58)$$

So, when input base current is zero the collector current $(1 + \beta)$ times I_{CO}. This current cannot be neglected. For transistor to operate in cut off region I_C should be almost equal to I_{CO}. To achieve this condition a small reverse biasing voltage is applied across base-emitter junction. The base emitter voltages for driving BJT in cutoff in CE configuration is as under,

$$V_{BE,\ cutoff} = -0.1\ V \ ;\ \text{for Ge} \quad (59)$$
$$= 0 \quad ;\ \text{for Si.}$$

In short, for driving the BJT in cutoff region in CE mode the emitter current $I_E = 0$, collector current $I_C = I_{CO}$, base current $I_B = -I_{CO}$ and $V_{BE} = -0.1$ for Ge and $V_{BE} = 0$ V for Si in npn transistors. Therefore, both junctions are reverse biased in cutoff region of operation of CE mode of operation of BJT.

Effect of temperature on I_{CO} :

The collector current in cutoff region I_{CO} is also denoted by I_{CBO}. It is called leakage current between base and collector under cutoff with emitter terminal open circuited. The leakage current between base and collector I_{CBO} doubles for every 10º rise in temperature for both Silicon and Germanium.

$$\therefore \quad \boxed{I_{CBO_2} = I_{CBO_1} 2^{\frac{(T_2 - T_1)}{10}}} \quad (60)$$

Collector to base reverse saturation current *i.e.* I_{CBO} is of order of micro-amperes for germanium and it is of order of nano-amperes for silicon. Because of this characteristic silicon is suitable up to higher temperature up to the order of 200°C where as Germanium is suitable up to 100°C.

Example 10

Leakage current approximately doubles for every 10°C increase in temperature of a silicon transistor. If a silicon transistor has I_{CEO} = 1000 nA at 30°C, what is its leakage current at 90°C?

(a) 32 µA (b) 64 µA

(c) 16 µA (d) 128 µA

IES(E&T,15)

Solution: Ans (b)

If leakage current of BJT doubles for every 10°C rise in temperature, the I_{CEO} as function of temperature is given by,

$$I_{CEO2} = I_{CEO1} 2^{\frac{T_2 - T_1}{10}}$$

Given, $T_1 = 30°C, T_2 = 90°C$

$I_{CEO1} = 1000$ nA

$$\Rightarrow \qquad I_{CEO2} = 1000 \times 2^{\frac{90-30}{10}} \text{ nA} = 2^6\ \mu\text{A} = 64\ \mu\text{A}$$

3. **Saturation region:** A BJT connected in CE configuration operates in saturation region when both emitter and collector junctions are forward biased. In the saturation region the collector current is almost independent of the base current. In this region transistor behaves like closed switch. The minimum base current required to drive a BJT to saturation can be given by,

$$I_{B,min} = \frac{I_{C,sat}}{h_{FE}} \tag{61}$$

Thus, a BJT enters into saturation region when

$$\boxed{I_B > \frac{I_{C,sat}}{h_{FE}}} \tag{61a}$$

Where, $h_{FE} = \beta$ = dc current gain of BJT and $I_{C,sat}$ is collector current at saturation. The collector current at saturation is given by,

$$I_{C,sat} = \frac{V_{CC} - V_{CE,sat}}{R_C} \tag{62}$$

The resistance offered by transistor in saturation region is called saturation resistance and it is given by

$$R_{CE,sat} = \frac{V_{CE,sat}}{I_C} \tag{63}$$

Overdrive factor :

Overdrive factor is BJT is the ratio of actual collector current to the collector current at the boundary of active and saturation region. Alternatively, overdrive factor can also be defined as the actual base current to the minimum base current required to drive the BJT to the saturation. Mathematically,

$$\text{Overdrive factor} = \frac{I_C}{I_{C,sat}} = \frac{I_B}{I_{B,min}} \tag{64}$$

Higher value of overdrive factor means the BJT is driven to deeper saturation.

Effect of temperature on $V_{BE,sat}$ and $V_{BC,sat}$:

In saturation region both emitter and collector junctions are forward biased so the voltages $V_{BE,sat}$ and $V_{BC,sat}$ has temperature co-efficients same as that of a forward biased pn junction. The temperature co-efficient of both $V_{BE,sat}$ and $V_{BC,sat}$ is –2.5 mV/°C. Therefore, the variations of $V_{BE,sat}$ and $V_{BC,sat}$ w.r.t. temperature can be given by,

$$\therefore \qquad \boxed{\frac{\partial V_{BE\,sat}}{\partial T} = -2.5\,\text{mV}/^{o}\text{C}} \tag{65}$$

$$\frac{\partial V_{BC\,sat}}{\partial T} = -2.5\,mV/^{o}C \qquad (65a)$$

Note : i. The temperature co-efficient of $V_{CE,sat}$ is approximately one tenth of that of $V_{BE,sat}$ and $V_{BC,sat}$
ii. Both α and β increases with increase in temperature.

Junction Voltages and Collector Current under different modes:

The variation of collector current of npn BJT against V_{BE} can be drawn as shown in Fig. 18

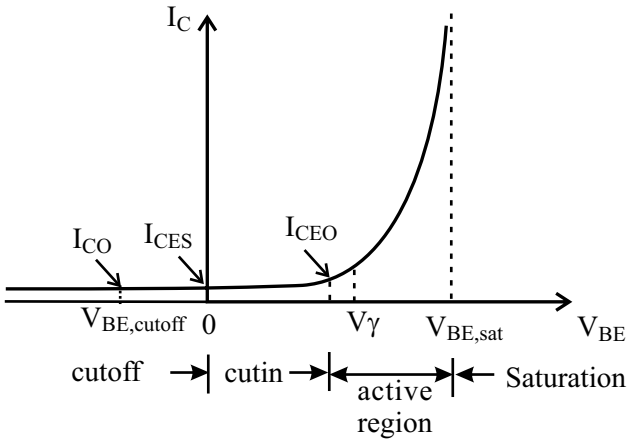


Fig. 18 Variation of collector current against base to emitter voltage

Cutoff : It is observed from Fig. 18 that when for cutoff region a $I_E = 0$, $I_C = I_{CO}$ and a reverse voltage of $V_{BE,cutoff} = -0.1$ V for Germanium and $V_{BE,cutoff} = 0$ V for Si is required.

Short Circuited Base : If base terminal of BJT is short circuited with emitter then voltage $V_{BE} = 0$ and collector current $I_C = I_{CES}$ and the current I_{CES} is almost same as I_{CO}.

Open Circuited Base : If base terminal is open circuited so that $I_B = 0$ then the collector current is equal to I_{CEO}. The current $I_{CEO} = (1+\beta)I_{CO}$. In case of Ge I_{CO} is of order of micro-amperes and it it is of order of nano-amperes for Si. So, the current I_{CEO} almost 10 times I_{CO} for Ge and almost same as I_{CO} for Si.

Cut-in Voltage (V_γ): It is threshold base-emitter voltage (V_{BE}) above which the BJT enters into the active mode of operation. The cut-in voltage is defined as the threshold base-emitter voltage at which collector current reaches the 1% of its maximum (saturation) value. It is 0.1 V for Ge and 0.5 V for Si.

Saturation voltages (V_σ) : The saturation voltage is limiting value of base-emitter voltage ($V_{BE,sat}$) behind which the transistor enters in the saturation mode of operation.

The typical values of transistor voltages are summarized in the table 1 given below,

Table 1 Values of junction voltages of npn BJT

	$V_{BE,cutoff}$	$V_{BE,cutin}$	$V_{BE,active}$	$V_{BE,sat}$	$V_{CE,sat}$
Si	0	0.5	0.7	0.8	0.2
Ge	–0.1	0.1	0.2	0.3	0.1

Operating Point or Q-Point:

Operating point of BJT connected in CE configuration is the point of intersection of load line and output characteristics corresponding to base current (I_B) of the circuit. It is also called Q-point. At Q-point $V_{CE} = V_{CEQ}$ and $I_C = I_{CQ}$. So, co-ordinates of Q point on output characteristics are represented by (V_{CEQ}, I_{CEQ}). The operating point of transistor shifts along the load line with variation of I_B. For amplifier application, the Q-point should be located almost at the mid of the load line in the active region. For switching application, the Q-point shifts between saturation and cut-off regions.

i. If Q-point is located near the saturation region, positive half of output current I_C is clipped-off or distorted.
ii. If Q-point is located near the cut-off region negative half of collector current I_C is distorted.
iii. Due to non-linearity in output characteristics in the active region of operation the variation in collector current are not equal for equal variation in base current. Therefore, the output current at collector is not directly proportional to the base current in the active region also. Thus the collector current is distorted even if transistor operated in active region with input base current purely sinusoidal. This distortion is called non linear distortion. Non linear distortion of transistor amplifier is measured in terms of total harmonic distortion (THD). Therefore, output of a transistor amplifier has multiple harmonics even if input signal is purely sinusoidal.

Base Spreading Resistance ($r_{bb'}$)

The dc resistance offered by the base of transistor under normal conditions of biasing is called base spreading resistance. Since area of cross section of base through which current flows from emitter region to base terminal is smaller than area of cross section of emitter and collector, therefore base spreading resistance is more than the resistance of emitter and collector. It is of order of 100 Ω.

Current gains of common emitter configuration :

1. dc current gain:

The dc current gain of CE configuration is defined as ratio of I_C to I_B.

$$\beta_{dc} = h_{FE} = \frac{I_C}{I_B} \tag{66}$$

Note : The dc current gain initially increases then decreases with increase in collector current of BJT.

2. Small signal current gain

The small signal gain of CE configuration is defined as ratio of differential change in collector current to differential change in base current with fixed collector to emitter voltage V_{CE}.

$$h_{fe} = \left.\frac{\partial i_c}{\partial i_b}\right|_{V_{CE} = \text{constant}} \tag{67}$$

Note : $h_{fe} > h_{FE}$ *for small currents and* $h_{fe} > h_{FE}$ *for large currents*

3. Large signal current gain

The large signal gain of CE configuration is obtained from the relation collector current with base current as under,

$$I_C = \beta I_B + (1 + \beta)\, I_{CO} \tag{68}$$

$$\beta = \frac{I_C - I_{CO}}{I_B + I_{CO}} = \text{Large signal current gain} \tag{69}$$

If I_{CO} is neglected then $\beta = \beta_{dc}$

Note : **Important parameters of CE configurations**

1. **Input impedance:** *Input impedance is medium (≈800 Ω)*
2. **Output impedance:** *Output impedance is high (≈50 kΩ)*
3. **Current gain:** *Current gain is high (≈80)*
4. **Voltage gain:** *Voltage gain is high (≈500)*
5. **Input and Output signals:** *Input and output signals are 180° out of phase. Therefore, common emitter configuration can be use as an inverter.*
6. **Leakage current:** *Leakage current is large (≈500 μA for Ge and ≈20 μA for Si).*

Note : *i. Common emitter configuration is mostly used as an amplifier in audio frequency range.*

ii. The BJT is operated in cutoff and saturation regions for switching and digital logic applications.

3.7.3 Common Collector Configuration

The output it taken from emitter and input form base of the transistor in common collector configuration. The common collector configuration is also known as emitter follower. The collector is connected to DC biasing voltage source only as shown in Fig.19

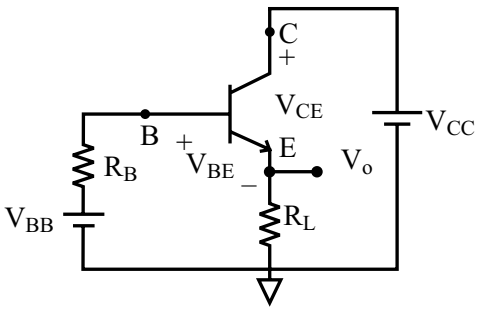


Fig. 19 Common collector configuration of npn transistor

Important parameters of common collector configuration:

1. Common collector configuration has high input impedance (i.e. 750 kΩ which is highest).
2. Output input impedance is low (about 50Ω which is lowest).
3. High current gain (about 100).
4. Voltage gain is almost unity but less than unity (about 0.95).
5. Leakage current is very large.
6. Output signal is in phase with input signal.

Application of common collector configuration:

1. Common collector configuration has high input impedance and low output impedance, therefore, it can be used for impedance matching of high impedance source to low impedance load.
2. Since the voltage gain of common collector configuration is unity, therefore, the output voltage at emitter is almost same as the input voltage at base, because of this characteristic this configuration can be used as emitter follower.
3. As current gain of common collector high and voltage gain is unity so it can be used for buffer application to increase power level of the signal without changing the voltage level in digital circuits.
4. It is used for construction of Darlington pair to provide high current gain.

3.8 Ebers-Moll model of BJT

Ebers-Moll model of BJT is developed by using normal and inverse model operations of BJT. It consists of two ideal diodes connected back to back with reverse saturation currents and two dependent current controlled current sources shunting the ideal diodes. This model is developed in this section for a npn transistor as follows.

In normal mode of operation the emitter junction is forward biased and collector junction is reverse biased. The collector current of BJT in normal mode of operation is given by,

$$I_C = \alpha_N I_C + I_{CO}\left(1 - e^{\frac{V_{CB}}{\eta V_T}}\right) \quad (70)$$

where, α_N is current gain for normal mode and I_{CO} is reverse saturation current in collector junction. In inverse mode the collector junction is forward biased and emitter junction is reverse biased. The emitter current in inverse mode operation of BJT is given by,

$$I_E = \alpha_I I_C + I_{EO}\left(1 - e^{\frac{V_{EB}}{\eta V_T}}\right) \quad (71)$$

Where α_I is current gain for inverse mode and I_{EO} is reverse saturation current in emitter junction. The parameters and are not independent rather they are related as under,

$$\alpha_I I_{EO} = \alpha_N I_{CO} \quad (72)$$

The current gain α_N in normal active mode is more than the current gain α in inverse active mode. By using equations (70) and (71), the Ebers-Moll model of BJT can be represented by two diodes connected back to back as shown in Fig.20.

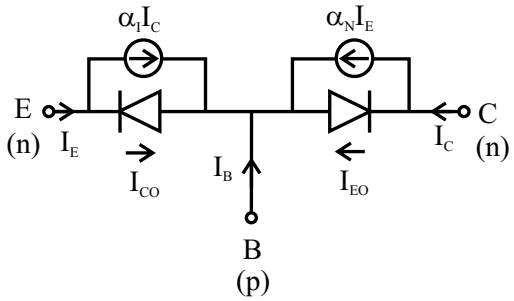


Fig. 20 Ebers-Moll model of npn transistor

Similarly, the Ebers-Moll model of pnp BJT can be drawn in Fig. 21.

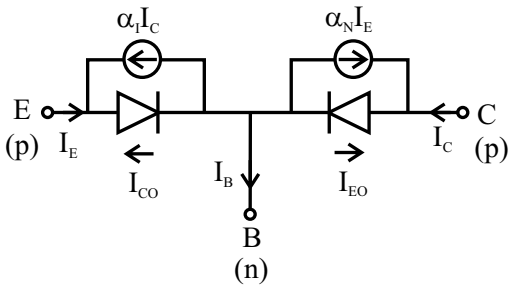


Fig. 21 Ebers-Moll model of pnp transitor

Note : *i. Ebers-Moll model is applicable for all modes i.e. forward active, saturation, cutoff and inverse active modes of operation of BJT.*

ii. When two simple diodes are connected back to back the combination cannot work like BJT because the resulting base width will be more than the diffusion length of minority carriers, so the amplifier gain 'α' will be negligible.

3.9 Non-Ideal Effects in BJT

1. Base Width Modulation

When collector junction of BJT is reverse biased in forward active mode the width of depletion layer at collector junction is increased and hence effective width of base is decreased This effect is known as *base width modulation or Early effect*. The edge of depletion layer on collection junction in base region penetrates in base.

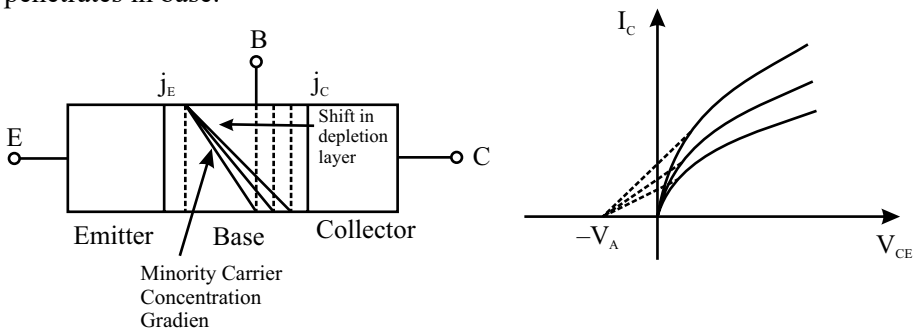


Fig. 22 Base width modulation and its effect on collector current

As concentration of injected minority carriers in base region becomes zero at edge of depletion layer in reverse biased collected junction so gradient of minority carriers in creases due to shifting of edge of depiction layer in base region. The collector current is directly proportional to concentration gradient of minority carriers in base region as already discussed in section 5. So, collector current increases with increase in voltage V_{CE} in output characteristics of CE configuration of BJT. If output characteristics of common emitter configuration of BJT are extended back ward all the lines meet at a point $-V_A$ on V_{CE} axis. The voltage $|V_A|$ is called early voltage.

If the early effect is also taken into account the collector current becomes,

$$I_C = I_S e^{V_{BE}/V_T}\left(1+\frac{V_{CE}}{V_A}\right)$$

The early effect gives rise to the output resistance of a BJT which is given by,

$$r_o = \left(\frac{\partial I_C}{\partial V_{CE}}\right)^{-1} = \left(I_S e^{V_{BE}/V_T} \times \frac{1}{V_A}\right)^{-1} = \frac{V_{CE} + V_A}{I_C} \quad (73)$$

$$r_0 = \frac{V_A}{I_C'} \quad (73a)$$

Where, $I_C' = I_S e^{V_{BE}/V_T}$ = collector current without early effect

2. Breakdown

The breakdown voltages of BJT decides the maximum voltage rating of BJT. The maximum reverse voltage rating at emitter junction is decided by Zener breakdown of emitter junction and maximum voltage at collector junction is decided by the avalanche multiplication as well avalanche breakdown of the collector junction. There are two mechanisms of breakdown of BJT at collector junction.

A. Punch Through Voltage

First breakdown occurs due to punch through phenomenon. When whole of the metallurgical width of base region of BJT is entirely covered by depletion layer of the collector junction by reverse biasing voltage V_{CB}, the condition is known as punch through. The increase in reverse biasing voltage at collector function beyond punch through voltage results in decrease in effective potential barrier at the emitter junction which in turn results in large in increase in minority carrier injection from emitter and hence excessive emitter current and collector current.

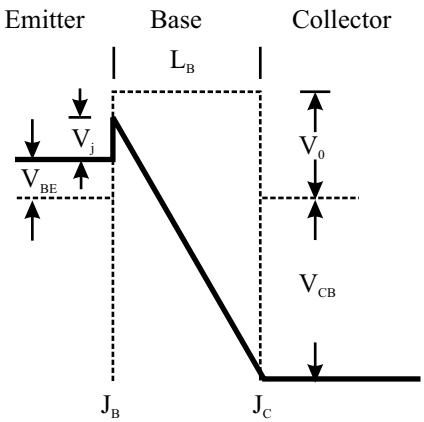


Fig. 23 Decrease in potential barrier due to punch through

The expression of width of depletion layer on one side of a pn junction was derived in pn junction diode. Similarly, the width of depletion layer in the base region at collector junction is obtained similar to width of depletion layer in a pn junction diode and it is given by,

$$W_{dB} = \sqrt{\frac{2\varepsilon}{q} \cdot \frac{N_C}{N_B} \cdot \frac{1}{N_C + N_B}\left(V_o + V_{CB}\right)} \quad (74)$$

Where the N_C is doping concentration in collector and N_B is doping concentration in the collector

region, V_o is potential barrier of unbiased junction and V_{CB} is reverse biasing voltage at the collector junction.

Fig. 24 shows the metallurgical width of base region (L_B), neutral width of base region (W_B) and width of depletion layer in base region at collector junction (W_{dB}).

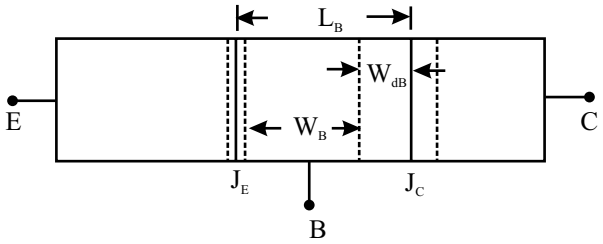


Fig. 24 Depletion layer width at collector junction in base region

The width of depletion layer at emitter junction is negligible. Therefore, at condition of punch through the width of depletion layer at collector junction becomes equal to the metallurgical width of base.

$$\therefore \quad W_{dB} = L_B \text{ and } V_{CB} = V_P$$

$$\Rightarrow \quad L_B = \sqrt{\frac{2\varepsilon}{q}\frac{N_C}{N_B}\cdot\frac{1}{N_C+N_B}\cdot\left(V_o + V_{CB}\right)} \tag{75}$$

At punch through $V_0 << V_p$ so $V_o + V_p \approx V_p$

$$\therefore \quad L_B = \sqrt{\frac{2\in}{q}\frac{N_C}{N_B}\cdot\frac{1}{N_C+N_B}\cdot V_p} \tag{76}$$

So, the voltage V_{CB} at punch through becomes as under,

$$\boxed{V_P = \frac{q L_B^{\,2}}{\varepsilon}\cdot\frac{N_B\left(N_C+N_B\right)}{N_C}} \tag{77}$$

B. Avalanche Multiplication Voltage

The second breakdown at collector junction is due to avalanche multiplication at high collector to base reverse biasing voltage. Let BV_{CBO} is breakdown voltage when emitter terminal is open circuit then the breakdown voltage when emitter terminal is open circuited is given by,

$$BV_{CEO} = \frac{BV_{CBO}}{\left(h_{FE}\right)^{1/n}} \tag{78}$$

or

$$BV_{CEO} = \frac{BV_{CBO}}{\beta^{1/n}} \tag{79}$$

Where n is a constant that varies from 2 to 10, for Ge 'n' is 6. The voltage BV_{CEO} is less then BV_{CBO} by a factor $\beta^{1/n}$. The collector current variation and breakdown voltages of BJT are shown in Fig. 25.

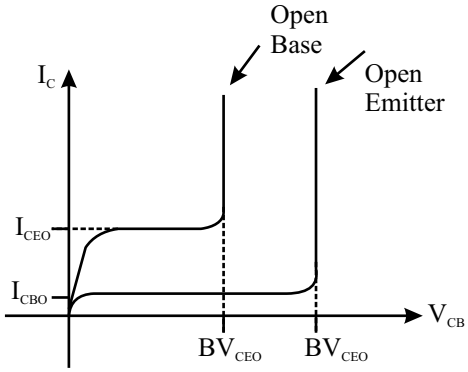


Fig. 25 Breakdown voltages of BJT

3. High Injection

When forward biasing voltage is increased the concentration of injected minority carriers from emitter is increased. A situation may arrive when minority carrier concentration at edge of depletion layer of emitter junction in the base region becomes more than majority carrier concentration of base, this situation is called high level injection. The high level injection results in increase in majority carrier concentration near the same edge of depletion layer in the base region in order to maintain electrical neutrality which in turns result increases the component of emitter current caused by injection of minority carriers from base to emitter region. High injection results in reduction of emitter injection efficiency. Thus over all emitter current is increased and current gain α and β are decreased. The change in BJT gain with respect to collector current is as shown in Fig.26

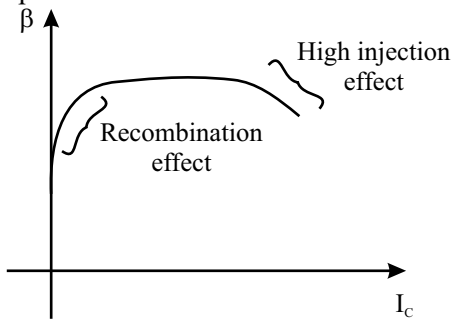


Fig. 26 Change of gain with change in collector current

At low current the gain decrease with decrease in current due to recombination effect and drop in gain at high current with increase in current is due to high injection effect.

Note : i. The collector current increase at slow rate with V_{BE} due to high injection as compassed to low level injection.

ii. The collector current in BJT is controlled either by base or emitter current so BJT is a current controlled device it.

4. Emitter Band gap Narrowing

When doping level of emitter is made excessively high there is spiting of discrete energy levels of donor atoms forming bands of energy which results in decrease in Band gap of emitter region. This effect results in reduction in emitter injection efficiency and increase in intrinsic concentration and

hence reduction in current gain of BJT.

3.10 Switching Characteristics of BJT

When a BJT is connected across the load resistance R_L in CE mode configuration it can be operated as a switch. The BJT behaves like an open switch when it is biased in cutoff region and it behaves like a closed switch when it is biased in saturation region. So, operation of BJT has to be changed from cutoff to saturation and vice versa in switching applications. Consider a BJT connected in CE mode is supplied with a pulse type of input signal such that its operation is confined to cutoff and saturation regions as shown in Fig. 27.

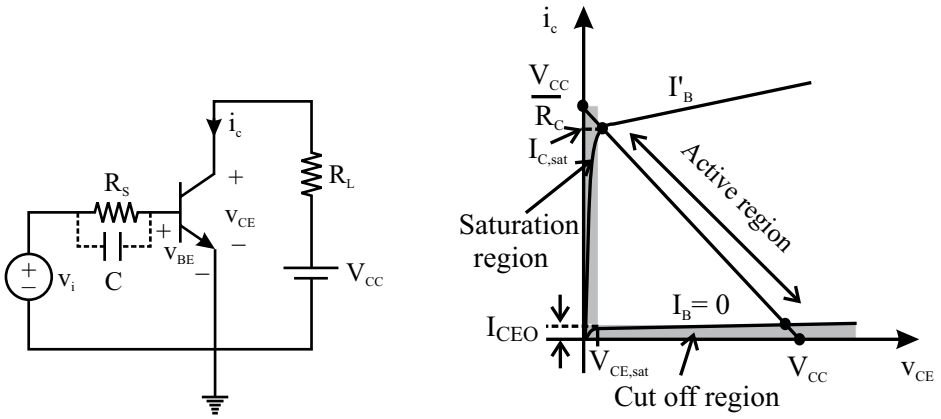


Fig. 27 BJT in CE mode operating in cutoff and saturation regions

Let, when input pulse is at $-V_1$ the transistor is in cutoff and at voltage V_2 the transistor is in saturation. When input pulse voltage is changed from $-V_1$ to V_2, the collector current does not immediately respond to the change input signal. Instead, there is time delay during which the collector current rises from 0 to 10% of tis maximum value, I_{cs} as shown in Fig. 28. This period is called delay time, t_d.

Delay Time (t_d):

The time delay is contributed by three factors , first time required for charging of emitter junction capacitance so that transistor is brought up from cutoff to active region, second time required for transit of minority carrier through the base region from emitter to collector junction and lastly the rise of collector current from 0 to $0.1I_{cs}$.

Rise Time (t_r) :

When collector current reaches 10% of its maximum value then more time required for collector current to rise from cutoff to saturation through active region from 10% to 90% of its maximum value. This period is known as rise time, t_r.

The sum of delay time, t_d and rise time, t_r is called turn ON time of BJT, $t_{ON} = t_d + t_r$. When input signal changes from V_2 to $-V_1$ the collector current again does not immediately respond to change in input signal. The interval between change of input signal from V_2 to $-V_1$ and decrease in collector current from maximum value to 90% of maximum value is called storage time, t_s.

Storage Time (t_s):

The storage time is the time required for removal excess minority carriers stored in the base region. If a BJT is driven in deep saturation the storage time may be 2 to 3 times of the rise or fall time which increases the turn off time of BJT and hence it put limitations of BJT in high frequency switching applications. The storage time can be reduced by connecting a properly selected capacitor across the base resistor which is shown by dotted lines in Fig.27(a). The storage time of BJT during turning off process is followed by fall time, t_f which the time required to fall the collector current from 90% to 10% of its maximum value.

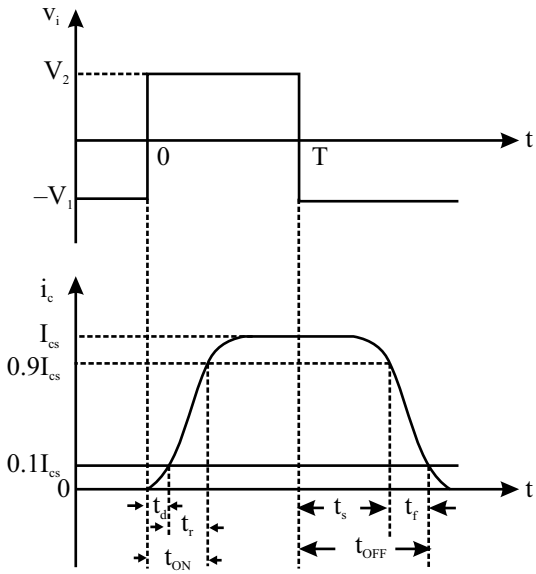


Fig. 28 Switching characteristics of BJT

Fall Time (t_f):

The fall time is the time during which the expansion of depletion layer and charging of transition capacitances at emitter and collector junctions takes place. The sum of storage time and fall time is called turn off time of BJT, $t_{OFF} = t_s + t_f$. In over saturation the collector current does not increase significantly but excess charges stored in base region are increased due to which the storage time of device is increased and hence the turn off time of BJT is increased resulting in limitation on use of BJT at high switching frequencies.

3.11 Schottky Clamped Transistor

The switching speed of a BJT can be increased by connecting a schottky diode between base and collector terminals of BJT as shown in Fig. 29. A BJT with Schottky diode connected between collector and base is called Schottky clamped transistor. The Schottky diode clamped between base and collector terminals reduces the storage time of the BJT. In forward active mode and cutoff mode B-C junction of BJT is reverse biased and Schottky diode is also reverse biased so the BJT works like normal transistor. However, when B-C junction is forward biased the voltage across the junction is clamped by Schottky diode at a level equal to the forward voltage drop of the diode which almost half of forward voltage of collector junction. So, the Schottky diode provides a path for excess base current and hence excess minority carriers stored in base region flow through Schottky diode instead of collector junction.

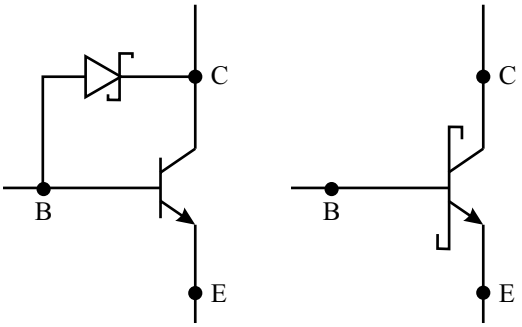
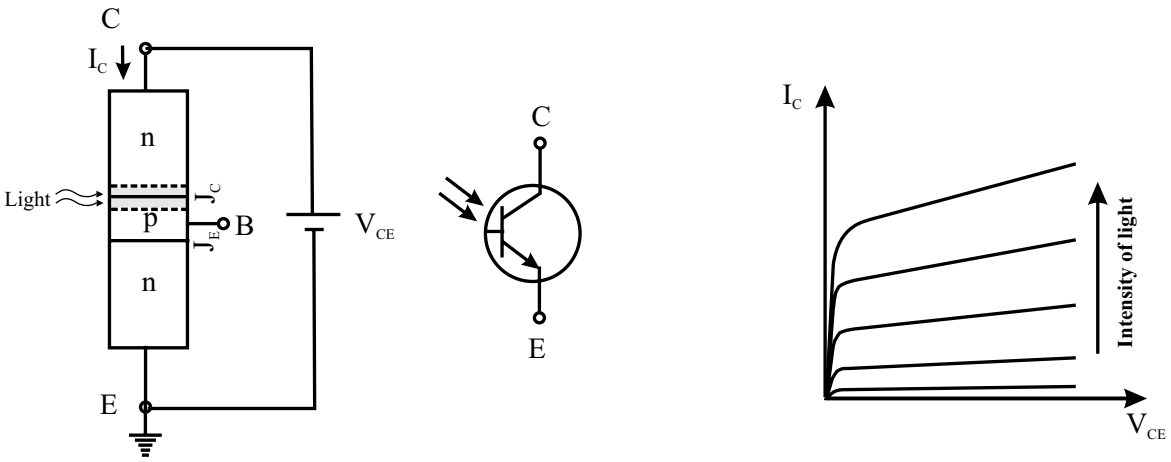


Fig. 29 Schottky clamped transistor

Since, voltage drop of diode is directly appearing across B-C junctions so the voltage V_{BC} of BJT is also reduced from 0.5 V to 0.3 V. The excess minority carrier in base region of npn BJT are directly proportional to $e^{V_{CB}/V}$ so reduction in voltage V_{CB} results in reduction of excess minority carriers stored in the base region and hence storage time of BJT is reduced. Since turnoff time of BJT is sum of storage time and fall time therefore, reduction in storage time results in reduction in turnoff time. The reduction turnoff time increases the switching frequency of BJT. Thus, the Schottky diode helps in avoidance of hard or deep saturation of BJT.

3.12 Phototransistor

A phototransistor has three layers similar to simple bipolar junction transistor. The base of phototransistor is kept open circuited. The collector-base junction of phototransistor is illuminated with a light of suitable wavelength. The collector junction of phototransistor is reverse biased where as emitter junction is slightly forward biased when base terminal is open circuited.



(a) Block diagram **(b) Symbol** **(d) Output charaterisics**

Fig. 30 : Block diagram, symbol and output characteristics of phototransistor

When the collector junction is not illuminated a reverse saturation current called dark current flows across the collector junction due jumping of thermally generated minority carriers across the junction i.e. due to jumping of holes from n-type collector and electrons from p-type in npn phototransistor. A phototransistor is more sensitive as compared to a photodiode. A phototransistor is most commonly used in common emitter configuration. The schematic diagram showing connnection of phototransistor along with symbol of phototransistor is shown in Fig.30. The collector current of phototransistor with no illumination of collector junction is given by,

$$I_C = (1+\beta)I_{CO} \tag{80}$$

If collector junction is illuminated with a light of suitable wavelength then there is generation of electron-hole pairs in the junction area and more holes jump from collector to base and more electrons from base to collector resulting in increase in reverse saturation collector current. The increase in collector current due to illumination is proportional to the intensity of incident light. If I_L is component collector current due to illumination then total collector current is given by,

$$I_C = (1+\beta)\,(I_{CO} + I_\lambda) \tag{81}$$

where I_λ is photo-generated current.

❐❐❐

GATE PRACTICE QUESTIONS

Q.1 In a uniformly doped BJT, assume that N_E, N_B and N_C are the emitter, base and collector doping in atoms/cm^3, respectively. If the emitter injection efficiency of the BJT is close to unity, which one of the following conditions is TRUE?

(a) $N_E = N_B = N_C$
(b) $N_E >> N_B$ and $N_B > N_C$
(c) $N_E = N_B$ and $N_B < N_C$
(d) $N_E < N_B < N_C$

GATE(EC/2010/2M)

Q.2 Consider the following statements S_1 and S_2.

S_1 : The β of a bipolar transistor reduces if the base width is increased.

S_2 : The β of a bipolar transistor increases if the doping concentration in the base is increased.

Which one of the following is correct?

(a) S_1 is FALSE and S_2 is TRUE
(b) Both S_1 and S_2 are TRUE
(c) Both S_1 and S_2 are FALSE
(d) S_1 is TRUE and S_2 is FALSE

GATE(EC/2004/1M)

Q.3 A BJT is said to be operating in the saturation region if

(a) Both the junctions are reverse biased
(b) Base-emitter junction is reverse biased and base collector junction is forward biased
(c) Base-emitter junction is forward biased and base collector junction reverse-biased
(d) Both the junction are forward biased

GATE(EC/1995/1M)

Q.4 If a transistor is operating with both of its junctions forward biased, but with the collector base forward bias greater than the emitter - base forward bias, then it is operating in the

(a) forward active mode
(b) Reverse saturation mode
(c) Reverse active mode
(d) Forward saturation mode

GATE(EC/1996/1M)

Q.5 If both the junctions of a transistor are forward biased, it will be in

(a) Saturation mode
(b) Active mode
(c) Cut off mode
(d) None

GATE(IN/2000/1M)

Q.6 A bipolar junction transistor (BJT) is used a power control switch by biasing it in the cut-off region (OFF state) or in the saturation region (ON state). In the ON state, for the BJT

(a) both the base-emitter and base-collector junctions are reverse biased
(b) the base-emitter junction is reverse biased, and the base-collector junction is forward biased
(c) the base-emitter junction is forward biased, and the base-collector junction is reverse biased
(d) both the base-emitter and base-collector junctions are forward biased

GATE(EE/2004 | 1 M)

Q.7 When a bipolar junction transistor is operating in the saturation mode, which one of the following statements is TRUE about the state of its collector-base (CB) and the base-emitter (BE) junctions?

(a) The CB junction is forward biased and the BE junction is reverse biased

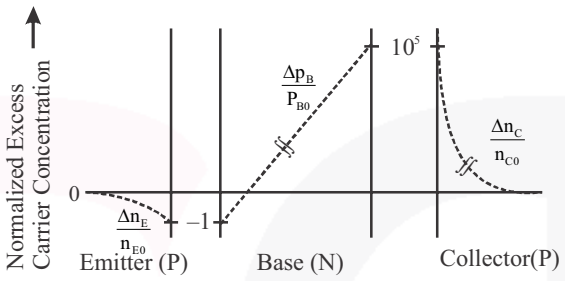
(b) The CB junction is reverse biased and the BE junction is forward biased

(c) Both the CB and BE junctions are forward biased

(d) Both the CB and BE junctions are reverse biased.

GATE(EC-II/2015/1M)

Q.8 For a narrow base PNP BJT, the excess minority carrier concentration (Δn_E for emitter, Δp_B for base. Δn_C for collector) normalized to equilibrium minority carrier concentration (n_{E0} for emitter, p_{B0} for base, n_{C0} for collector) in the quasi-neutral emitter, base and collector regions are shown below. Which one of the following biasing modes is the transistor operating in?



X and Y axes are not to scale

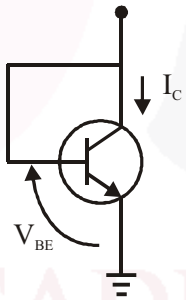
(a) Forward active

(b) Saturation

(c) Inverse active

(d) Cutoff

Q.9 For an npn transistor connected as shown in figure V_{BE} = 0.7 Volts. Given that reverse saturation current of the junction at room temperature 300°K is 10^{-13} A, the emitter current is



(a) 30 mA

(b) 39 mA

(c) 49 mA

(d) 20 mA

GATE(EC/2005/2M)

Q.10 Which of the following statements are correct for basic transistor amplifier configurations ?

(a) CB amplifier has low input impedance and a low current gain.

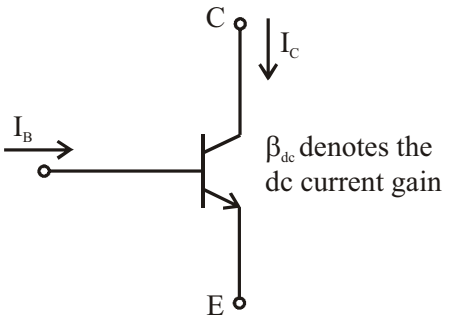
(b) CC amplifier has low output impedance and a low current gain.

(c) CE amplifier has very poor voltage gain but very high input impedance.

(d) The current gain of CB amplifier is higher than the current gain of CC amplifier.

GATE(EC/1990/2M)

Q.11 If the transistor in Figure is in saturation, then



(a) I_C is always equal to $\beta_{dc}I_B$
(b) I_C is always equal to $-\beta_{dc}I_B$
(c) I_C is greater than or equal to $\beta_{dc}I_B$
(d) I_C is less than or equal to $\beta_{dc}I_B$

GATE(EC/2002/1M)

Q.12 If for a silicon n-p-n transistor, the base-to-emitter voltage (V_{BE}) is 0.7 V and the collector-to-base voltage (V_{CB}) is 0.2 V, then the transistor is operating in the

(a) normal active mode
(b) saturation mode
(c) inverse active mode
(d) cutoff mode

GATE(EC/2004/1M)

Q.13 Choose the correct match for input resistance of various amplifier configurations shown below

Configuration	***Input resistance***
CB : Common Base	LO : Low
CC : Common Collector	MO : Moderate
CE : Common Emitter	HI : High

(a) CB-LO, CC-MO, CE-HI
(b) CB-LO, CC-HI, CE-MO
(c) CB-MO, CC-HI, CE-LO
(d) CB-HI, CC-LO, CE-MO

GATE(EC/2003/1M)

Q.14 The common-collector transistor configuration has the following properties :

(a) High input and Low output impedances
(b) High input and High output impedances
(c) Low input and Low output impedances
(d) Low input and High output impedances

GATE(IN/1994/1M)

Q.15 For a single BJT common base amplifier,

(a) current gain as well as voltage gain can be greater than unity
(b) current gain can be greater than unity,but voltage gain is always less than unity
(c) voltage gain can be greater than unity but current gain is always less than unity
(d) Current gain well as voltage gain is always less than unity

GATE(IN/2008/2M)

Q.16 An npn bipolar junction transistor (BJT) is operating in the active region. If the reverse bias across the base – collector junction is increased, then

(a) the effective base width increases and common – emitter current gain increases
(b) the effective base width increases and common – emitter current gain decreases
(c) the effective base width decreases and common – emitter current gain increases

(d) the effective base width decreases and common – emitter current gain decreases

GATE(EC-II/2017/1M)

Q.17 The Ebers-Moll model is applicable to

(a) Bipolar junction transistors
(b) NMOS transistors
(c) Unipolar junction transistors
(d) Junction field-effect transistors

GATE(EC/1995/1M)

Q.18 The Ebers-Moll model of a BJT is valid

(a) only in active mode
(b) only in active and saturation modes
(c) only in active and cut-off modes
(d) in active, saturation and cut-off modes

GATE(EC-II/2016/1M)

Q.19 The break down voltage of a transistor with its base open is BV_{CEO} and that with emitter open is BV_{CBO}, then

(a) $BV_{CEO} = BV_{CBO}$
(b) $BV_{CEO} > BV_{CBO}$
(c) $BV_{CEO} < BV_{CBO}$
(d) BV_{CEO} is not related to BV_{CBO}

GATE(EC/1995/1M)

Q.20 The common-emitter short-circuit current gain β of a transistor

(a) is a monotonically increasing function of the collector current I_C.
(b) is a monotonically decreasing function of I_c.
(c) increases with I_c, for low I_c, reaches a maximum and then decreases with further increase in I_c.
(d) is not a function of I_c.

GATE(EC/1996/1M)

Q.21 In a common emitter BJT amplifier, the maximum usable supply voltage is limited by

(a) Avalanche breakdown of base-emitter junction
(b) Collector-base breakdown voltage with emitter open (BV_{CBO})
(c) Collector-Emitter breakdown voltage with base open (BV_{CEO})
(d) Zener breakdown voltage of the Emitter-Base junction

GATE(EC/1997/2M)

Q.22 The early effect in a bipolar junction transistor is caused by

(a) fast turn-on
(b) fast turn-off
(c) large collector-base reverse bias
(d) large emitter-base forward bias

GATE(EC/1999/1M)

Q.23 The phenomenon known as "Early Effect" in a bipolar transistor to a reduction of the effective base - width caused by

(a) Electron - hole recombination at the base
(b) the reverse biasing of the base - collector junction
(c) the forward biasing of emitter - base junction
(d) the early removal of stored base charge during saturation-to-cutoff switching

GATE(EC/2006/1M)

Q.24 An increase in the base recombination of a BJT will increase

(a) the common emitter dc current gain β
(b) the breakdown voltage BV_{CEO}

(c) the unity-gain cut-off frequency f_T (d) the transconductance g_m

GATE(EC-II/2014/1M)

Q.25 If the base width in a bipolar junction transistor is doubled, which one of the following statements will be TRUE?

(a) Current gain will increase

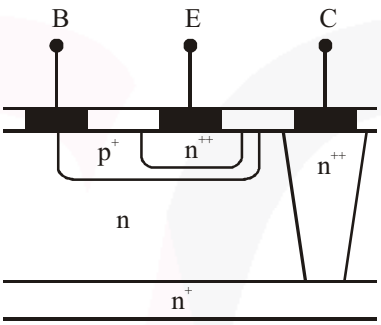
(b) Unity gain frequency will increase

(c) Emitter-base junction capacitance will increase

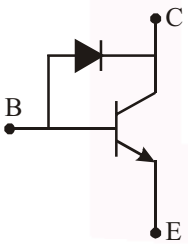
(d) Early voltage will increase

GATE(EC-III/2015/1M)

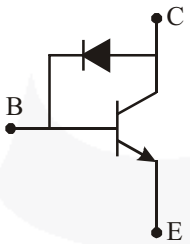
Q.26 The correct circuit representation of the structure shown in the figure is



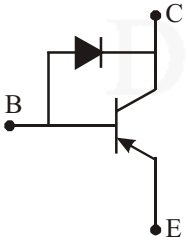
(a)



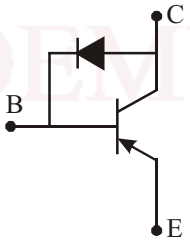
(b)



(c)

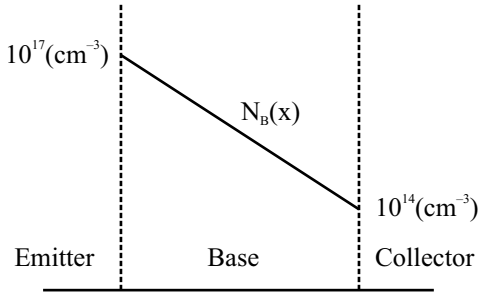


(d)



GATE(EC/2019/1M)

Q.27 The base of an npn BJT T1 has a linear doping profile $N_B(x)$ as shown below. The base of another npn BJT T2 has a uniform doping N_B of 10^{17} cm^{-3}. All other parameters are identical for both the devices. Assuming that the hole density profile is the same as that of doping, the common-emitter current gain of T2 is



(a) approximately 2.0 times that of T1
(b) approximately 0.3 times that of T1
(c) approximately 2.5 times that of T1
(d) approximately 0.7 times that of T1

GATE(EC/2020/2M)

❐❐❐

ANSWERS & EXPLANATIONS

Q.1 ***Ans.(b)***

For emitter injection efficiency of the BJT close to unity the doping level of emitter should be much higher than the base region. So, option (b) is correct.

Q.2 ***Ans.(d)***

S_1 : The common emitter gain, β, of BJT is given by,

$$\beta = \frac{I_C}{I_B}$$

When either base width is increased or doping in base region is increase the recombination rate in base region is also increased. The increase in recombination rate in the base region results in increase in base current and decrease in collector current. Therefore, current gain β reduces with increase in base width or doping level base region.

So, statement S_1 is true but S_2 is false.

Q.3 ***Ans.(d)***

A BJT operate in saturation region when both base-emitter and base collector junctions are forward biased.

Q.4 ***Ans.(d)***

A transistor operates in forward saturation mode when both emitter-base and base-collector junctions are forward biased.

Q.5 ***Ans.(a)***

A BJT operate in saturation region when both base-emitter and base collector junctions are forward biased.

Q.6 ***Ans. (d)***

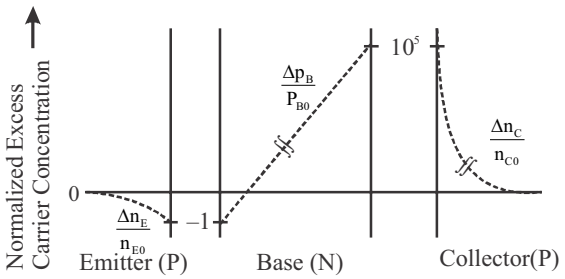
A BJT operate in saturation region when both base-emitter and base-collector junctions are forward biased.

Q.7 ***Ans. (c)***

A BJT operate in saturation region when both base-emitter and base collector junctions are forward biased.

Q.8 ***Ans. (c)***

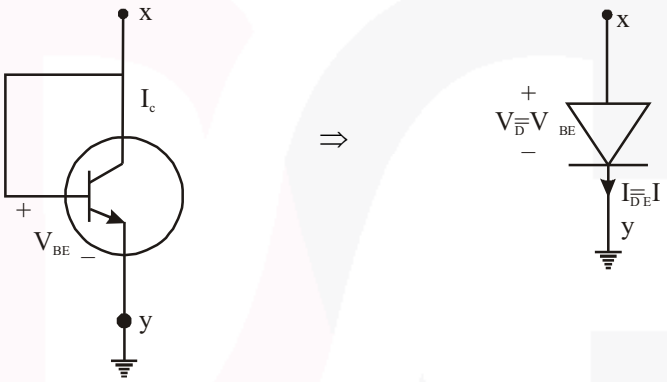
In forward active mode of operation the concentration of excess minority carriers is maximum at edges of depletion layer of emitter junction and zero at the edges of depletion layer of collector junction whereas in inverse active mode of operation the concentration of excess minority carriers is maximum at edges of depletion layer of collector junction and zero at the edges of depletion layer of emitter junction. In the given figure the concentration of excess minority carriers is maximum at edges of depletion layer of collector junction and zero at the edges of depletion layer of emitter junction. Therefore, the given BJT must be operating in inverse active mode.



X and Y axes are not to scale

Q.9 Ans.(c)

When collector terminal of BJT is shorted with base terminal it behaves like a diode with base emitter junction behaving like diode junction.



The diode current is given by,

$$I_D = I_O\left(e^{V_D/V_T} - 1\right)$$

Where, I_O = Reverse saturation current

$V_D = V_{BE}$ = Voltage across junction

$$V_T = \frac{T}{11600} = \text{Thermal voltage}$$

T = Temperature in ^oK

Given, $T = 300\ ^oK$, $I_O = 10^{-13}A$, $V_{BE} = 0.7\ V = V_D$

$$\therefore \quad V_T = \frac{300}{11600} \approx 0.026$$

$$\Rightarrow \quad I_D = I_E = 10^{-13}\left(e^{\frac{0.70}{0.026}} - 1\right) A \approx 49.2\ mA$$

Q.10 Ans (a)

Performance parameters of CB, CE and CC configuration of BJT,

Parameter	CB	CE	CC
1. Input Impedance	Low (22.5)Ω	Medium (1065)Ω	Very high (144 k)Ω
2. Output Impedance	Very High (1072)Ω	High (45.5 kΩ)	Low (80)Ω
3. Current gain	Low (less than unity)	High (–46.5)	High (47.5)
4. Voltage gain	High (131)	High (–131)	Low (Less than Unity)
5. Leakage current	Very small	Large For Ge 500 μA For Si 20 μA	Very large
6. Phase angle between input and output	Same phase	180° phase shift	Same phase

So, CB amplifier has low input impedance and low current gains.

Q.11 Ans.(d)

Minimum value of base current for transistor to enter into saturation,

$$I_{B,\,min} = \frac{I_C}{\beta} = \frac{I_C}{h_{EF}}$$

So, BJT enters into saturation region when,

$$I_B > I_{B,min}$$

or $$I_B > \frac{I_C}{\beta}$$

$\Rightarrow$ $$I_C < \beta I_B$$

Q.12 Ans.(a)

For forward biasing of p-n junction of Si the cut in voltage, V_γ is of order of 0.5 V

Given,

i. Base-to-Emitter junction voltage,

$$V_{BE} = 0.7\ V$$

Since $V_{BE} > V_\gamma$, so base to emitter junction is forward biased.

ii. Collector to base junction voltage,

$$V_{CB} = 0.2\ V.$$

Since $V_{CB} < V_\gamma$, so collector to base junction is not forward biased.

When B-E junction is forward biased and C-B junction is reverse biased the BJT operates is normal active mode.

Q.13 Ans.(b)

Performance parameters of CB, CE and CC configuration of BJT amplifiers,

Parameter	CB	CE	CC
1. Input Impedance	Low (22.5)Ω	Medium (1065)Ω	Very high (144 k)Ω
2. Output Impedance	Very High (1072)Ω	High (45.5 kΩ)	Low (80)Ω
3. Current gain	Low (less than unity)	High (–46.5)	High (47.5)
4. Voltage gain	High (131)	High (–131)	Low (Less than Unity)
5. Leakage current	Very small	Large For Ge 500 μA For Si 20 μA	Very large
6. Phase angle between input and output	Same phase	180° phase shift	Same phase

So, CB has low input impedance, CC has high input impedance and CE has moderate input impedance.

Q.14 ***Ans.(a)***

The common collector configuration of BJT has high input impedance, low output impedance and almost unity voltage gain.

Q.15 ***Ans.(c)***

For single BJT common base amplifier voltage gain can be greater than unity but current gain is always less than unity.

Q.16 Ans. (c)

An npn bipolar junction transistor (BJT) is operating in the active region. If the reverse bias across the base – collector junction is increased, then the effective base width decreases and common – emitter current gain increases due to the early effect.

Q.17 ***Ans.(a)***

Ebers-Moll model is applicable to BJT. It consists of two ideal diodes placed back to back with reverse saturation currents I_{EO} and $-I_{CO}$ and two dependent current controlled sources shunting the diodes.

Q.18 ***Ans. (d)***

The Ebers-Moll model of a BJT is valid for all four modes of operation of BJT i.e. forward active, inverse active, saturation and cut-off modes.

Q.19 ***Ans.(c)***

The relation between open base breakdown voltage (BV_{CEO}) of BJT with open emitter voltage (BV_{CBO}) is given by,

$$BV_{CEO} = BV_{CBO}\sqrt{\frac{1}{h_{FE}}}$$

As $h_{FE} > 1$ so BV_{CEO} is less than BV_{CBO}.

Q.20 Ans.(c)

The common-emitter short-circuit current gain β of a transistor increases with I_c, for low I_c, reaches a maximum and then decreases with further increase in I_c.

Q.21 Ans.(b)

In a common emitter BJT amplifier maximum usable supply voltage is limited by collector -base breakdown voltage with emitter open (BV_{CBO})

Q.22 Ans.(c)

The early effect in a bipolar junction transistor is caused by large collector-base reverse biased voltage which results in increase in width of depletion layer in base region and decrease in overall width of base region.

Q.23 Ans.(b)

The phenomenon of "Early Effect" in BJT is caused by reverse biasing voltage of base-collector junctions which results in base width modulation.

Q.24 Ans.(b)

The breakdown voltage BV_{CEO} of BJT with open base terminal is given by,

$$BV_{CEO} = BV_{CBO}\sqrt{\frac{1}{h_{FE}}}$$

where h_{FE} is dc gain and BV_{CBO} is breakdown voltage with emitter terminal open circuited. The increase in base recombination results in decreases in number of minority carriers reaching at collector junction and thus dc current gain h_{FE} of BJT is also decreased which in turn results in increase the breakdown voltage BV_{CEO}

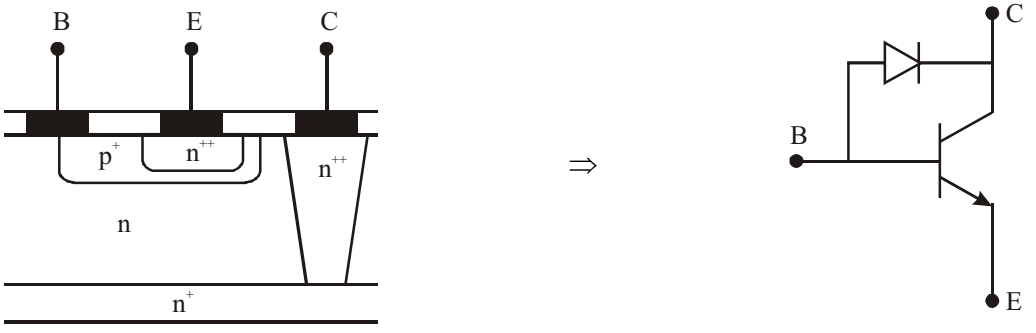
Q.25 Ans. (d)

The early voltage of BJT is given by,

$$V_P = \frac{q L_B^{\,2}}{\varepsilon} \cdot \frac{N_B\left(N_C + N_B\right)}{N_C}$$

So, the early voltage of BJT increases with increase in base width so if the base width in a bipolar junction transistor is doubled early voltage will increase.

Q.26 Ans.(a)



Observations from the given structure,

(i) Collector region is n-type with heavily doped n^{++} layer.

(ii) Emitter region is n-type with n^{++} layer.

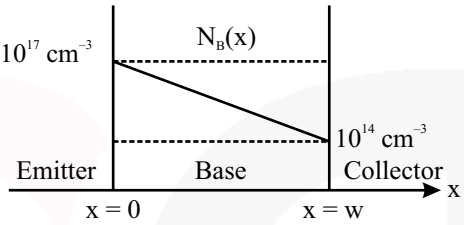
(iii) Base region has two doping p^{+} layer and n-layer.

(iv) So, there is npn BJT fabricated between n^{++}(C) to p^{+}(B) and n^{++} (E) layers

(v) There is additional unipolar junction n-n^{++} between collector and base which acts like a diode with n^{++} layer like cathode and n-layer like anode.

The equivalent circuit of given structure becomes as shown above.

Q.27 Ans(a)



For npn transistor collector current,

$$I_C \approx I_{nE}$$

The I_{nE} component of emitter current directly proportional to excess minority carriers concentration i.e. electrons stored in base region & inversely proportional to majority carrier charge of holes in base region.

$$\therefore \quad I_C \propto I_{AE} \propto \frac{1}{Q_B}$$

The majority carrier holes charge in base region can be given by

$$Q_B = \int_0^W N_B(x)\,dx$$

$$\therefore \quad I_C \propto \frac{1}{\int_0^W N_B(x)\,dx}$$

Collector current of BJT,

$$I_C \propto I_{nE} \propto e^{\frac{qV_{BE}}{kT}}$$

Common emitter gain β of BJT,

$$\beta = \frac{I_C}{I_B}$$

$$\Rightarrow \quad \beta \propto \frac{e^{\frac{qV_{BE}}{2kT}}}{e^{\frac{qV_{BE}}{kT}}} \propto e^{\frac{-qV_{BE}}{2kT}} \propto I_c^{-1}$$

$$\therefore \quad \frac{\beta_{T2}}{\beta_{T1}} = \frac{I_{C1}}{I_{C2}} = \frac{\int_0^W N_{B2}(x)dx}{\int_0^W N_{B1}(x)dx}$$

$$\frac{\beta_{T2}}{\beta_{T1}} = \frac{W \times 10^{17}}{W \times 10^{14} + \frac{1}{2}\left(10^{17} - 10^{14}\right) \times W} = \frac{10^{17}}{\frac{10^{17} + 10^{14}}{2}}$$

$$\Rightarrow \quad \frac{\beta_{T2}}{\beta_{T1}} = \frac{2 \times 10^{17}}{10^{17} + 10^{14}} \approx 1.998$$

$$\Rightarrow \quad \beta_{T2} = 1.998\ \beta_{T1}$$

❐❐❐

Ch 4 FETs And MOS Capacitors

4.1 Introduction

Field effect transistors are the semiconductor devices which operate on principle of control of output current by input voltage or electric field. The field effect transistors are of two types called Junction Field Effect Transistor (JFET) and Metal Oxide Semiconductor Field Effect Transistor (MOSFET). The current in FETs is contributed by one type of carriers only therefore these devices are unipolar devices. The field effect transistors have following advantages and disadvantages over bipolar junction transistor.

Advantages of FETs over BJT

1. Current in FET is carried by majority carriers, therefore, it is a unipolar devices but in BJT current is carried by both electron and holes, therefore, BJT is a Bipolar device.
2. FETs have very high input impedance of order of Mega ohms as compared to BJT
3. BJT is more noisy than FETs.
4. FET exhibits no offset voltage as observed in BJT.
   Offset voltage is the drop across the junction in BJT.
5. FETs suffer from no secondary breakdown like BJT. Thermal breakdown is called secondary breakdown where as Avalanche and zener breakdowns called primary breakdown.
6. FETs have very small switching losses as compare to BJT. But their ON state losses are more as compared to BJT.
7. Switching frequency of FETs is higher than BJT because their turn OFF time is smaller.
8. FETs have better frequency response than BJT.
9. The breakdown voltage of FETs has positive temperature coefficient that means breakdown voltage increases with increase in temperature. The positive temperature coefficient of FETs makes it suitable for parallel operation.

Disadvantages of FETs as compared to BJT

1. FETs have higher ON state losses because their resistance is more than that of BJT in continuous conduction state.
2. The dynamic resistance of FETs is higher as compared to BJT.
3. The gain bandwidth product of FETs is smaller as compared to BJT.

4.2 Metal-Oxide-Semiconductor (MOS) Capacitor (Only for ECE)

A Metal-Oxide-Semiconductor (MOS) capacitor has a a metal gate deposited on a oxide (SiO_2) layer. The oxide layer is fabricated on a semiconductor substrates as shown in Fig.1. The semiconductor

substrate can be either n-type or p-type. A Metal-Oxide-Semiconductor (MOS) capacitor is heart of MOSFET operation.

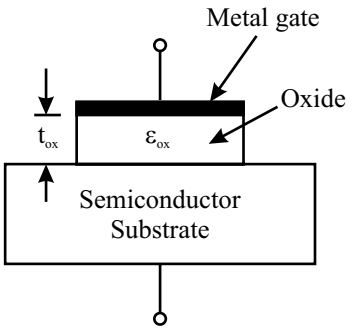


Fig.1 Structure of basic MOS capacitor structure

A MOS capacitor acts like a parallel plate capacitor with a dielectric inserted between the plates. The capacitor per unit area of the oxide of the MOS capacitor is given by,

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

where, ε_{ox} permittivity and t_{ox} is thickness of oxide layer.

A MOS capacitor can work in three modes of operations called accumulation mode, depletion mode and inversion mode of operations.

Accumulation mode

If gate terminal is given a potential such that there is accumulation of majority carriers of substrate at the interface of oxide and semiconductor then mode of operation is called accumulation mode.

Depletion Mode

If gate terminal of the MOS capacitor is given such a potential that it repels the majority carrier from the interface of oxide and semiconductor resulting in formation of depletion layer in the substrate region at the interface then the mode of operation is called depletion mode. In depletion mode there are induced space charge of impurity atoms of semiconductor substrate in the depletion layer.

Inversion Mode

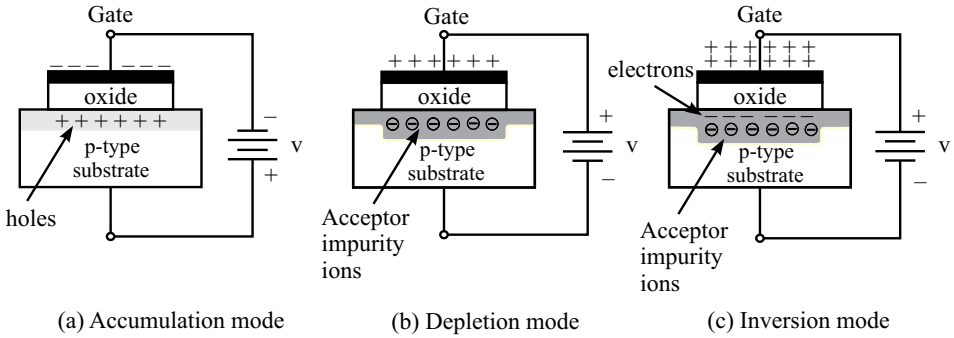
If gate terminal of the MOS capacitor is given such a potential that it attracts minority carries from semiconductor substrate at oxide-semiconductor interface forming an inversion layer with concentration of minority carriers at more than the concentration majority carriers in bulk of substrate then the mode of operation is called inversion mode. Inversion mode is key to operation of MOSFET. The critical gate voltage, when there is formation of inversion layer at the surface, is called threshold voltage.

A MOS capacitor offers maximum capacitance in accumulation and inversion modes of operations if high frequency effects are neglected. The capacitance offered is minimum in the depletion mode of operation.

4.2.1 Energy Band Diagram of MOS Capacitor

Case - I : MOS Capacitor with p-type substrate

The biasing of a MOS capacitor with p-type semiconductor substrate for accumulation, depletion and inversion modes of operation is shown in Fig. 2.



(a) Accumulation mode (b) Depletion mode (c) Inversion mode

Fig.2 Biasing of MOS capacitor with p-type substrate (a) accumulation mode (b) depletion mode (c) inversion mode

Energy band diagram under equilibrium

The work function of metal is normally defined as energy required to bring an electron on the surface or vacuum level from the Fermi level of the metal. However, for MOS capacitor and MOSFET the work function ($q\phi_m$) for metal-oxide interface will be defined as energy required to move the electron from Fermi level of metal to conduction band of oxide and work function ($q\phi_{sem}$) for oxide-semiconductor interface will be defined as energy required to move an electron from Fermi level of semiconductor to conduction band of the oxide. There is another important term $q\phi_F$ which will be used for difference in energy of actual Fermi level and intrinsic Fermi level for semiconductor. *Under idealized condition it is assumed that work of metal is equal to work function of the semiconductor (i.e.* $\phi_m = \phi_{sem}$ *) so that there is no difference in work functions.* The Fermi level under idealized conditions at equilibrium when no bias is applied to the MOS capacitor is as shown in Fig.3(a). At equilibrium with zero bias the Fermi level on both sides of oxide layer is at the same level.

Energy band diagram under accumulation mode

The MOS capacitor with p-type semiconductor substrate operates in accumulation mode when the metal gate is connected to negative terminal of the supply as shown inf Fig. 2(a). When gate terminal is connected to the negative potential the electrons are deposited on gate metal. The negative charge on the gate metal induces an electric field in the oxide layer which in turn attracts holes from the p-type semiconductor substrate and holes are accumulated on the oxide-semiconductor interface as shown in the Fig. 3(a). The applied negative potential on gate terminal results in increase in energy of electrons in metal. As a result Fermi level of metal E_{Fm} shifts above the equilibrium position (E_{Fs}) by qV, where V is applied voltage. The work function of metal ($q\phi_m$) and that of semi conductor ($q\phi_{sem}$) does not change with applied voltage so it results in tilting of conduction band of the oxide layer as shown in Fig. 3(b). The induced electric field $\mathcal{E}$ in oxide causes a gradient in intrinsic Fermi energy level E_i near the oxide-semiconductor interface. The induced electric field in oxide is related to the gradient in E_i as under,

$$\mathcal{E}(x) = \frac{1}{q}\frac{dE_i}{dx} \quad (1)$$

The accumulation of holes at oxide-semiconductor interface increases the concentration of holes at the interface. The increased concentration of holes at the interface in semiconductor results in upward bending of upper level of valence band (E_V) closer to the Fermi energy level(E_{Fs}) at the interface. Therefore, the upper energy level of valence band of semiconductor is tilted upward near the interface. Similar tilt is observed in intrinsic energy level as well as lowest energy level of conduction band of the semiconductor as shown in Fig. 3(b). The concentration of holes in valence band of a semiconductor in terms of actual Fermi level and intrinsic Fermi level is given by,

$$p = n_i e^{(E_i - E_{Fs})/kT} \quad (2)$$

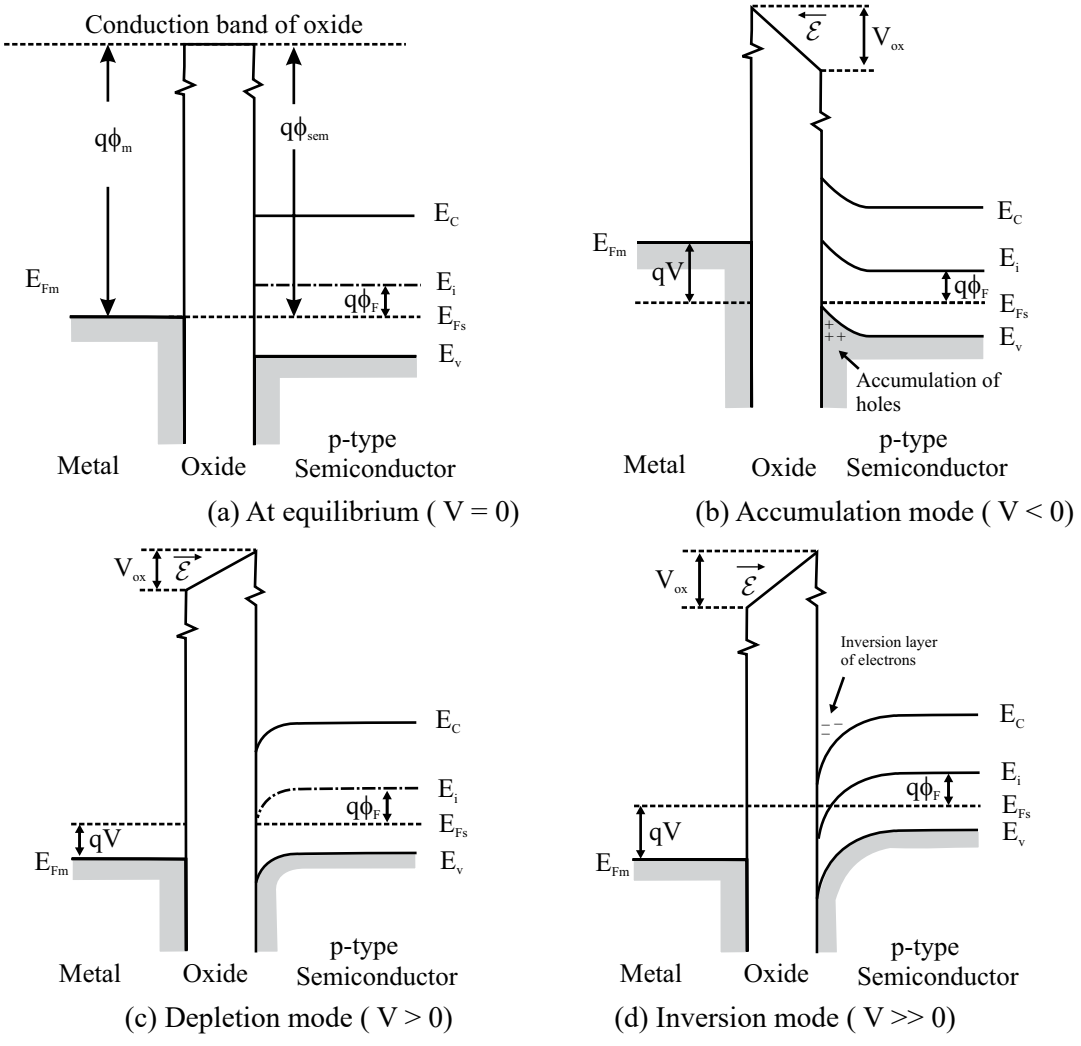


Fig.3 Energy band diagram of MOS with p-type semiconductor substrate (a) At thermal equilibrium (b) under accumulation mode (c) under depletion mode (d) under inversion mode

It is observed from equation (2) that concentration of holes near the oxide-semiconductor interface

can increase only if there is increase in difference $E_i - E_{Fs}$ near the interface. If there is no current in the semiconductor then there is no variation in Fermi level, E_{Fs}, in the semiconductor. So, the difference $E_i - E_{Fs}$ near the oxide-semiconductor interface is increased only by tilting the intrinsic level E_i upward at the interface. The Fermi level, E_{Fs}, at interface is more closer to the upper energy level of valence band which means holes concentration at interface is larger than that arising from the doping of p-type substrate.

Energy band diagram under depletion mode

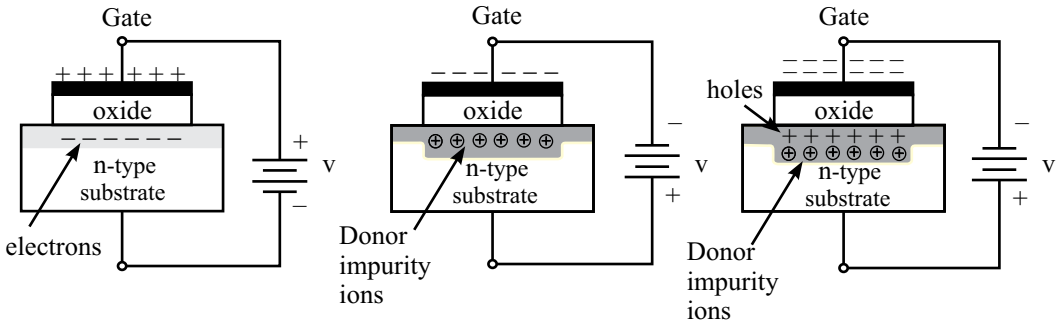
The MOS capacitor with p-type semiconductor substrate work in depletion mode when the metal gate terminal of the capacitor is given a small positive potential as shown in Fig. 2(b). When gate terminal is connected to a small positive potential the gate metal acquires a positive charge. The applied positive potential on gate terminal results in decrease in energy of electrons in metal. As a result Fermi level of metal E_{Fm} shifts down the equilibrium position (E_{Fs}) by qV, where V is applied voltage. The positive charge on the gate metal induces an electric field in the oxide layer which repels the holes away from oxide-semiconductor interface and, therefore, a depletion layer is formed below the gate region close to oxide-semiconductor interface as shown in Fig. 3(c). The depletion region near the interface consists of uncovered bound negative charges of acceptor impurity just like the depletion region of pn junction. The depletion of holes near the oxide-semiconductor interface results in decrease in concentration of holes which in turn results in tilting of upper energy level of valence band (E_V) away from the Fermi level (E_{Fs}) near the interface in depletion region as shown in Fig. 3(c). Similar tilt is observed in intrinsic energy level as well as lowest energy level of conduction band of the semiconductor.

Energy band diagram under inversion mode

When positive potential, connected to the metal gate, is further increased there is a situation when intrinsic Fermi level E_i bends below the Fermi level E_{Fs} at oxide-semiconductor interface and the lowest level of conduction band (E_C) also bends downward and becomes closer to the Fermi level (E_{Fs}) as compared to highest level of valence band (E_V) as shown in Fig. 3(d). Therefore, the region near oxide-semiconductor interface has properties similar to that of a n-type semiconductor. This bending of E_i below E_{Es} at oxide-semiconductor result in large electron concentration in conduction band near oxide-semiconductor interface. For inversion mode bend in intrinsic level at surface, $\phi_s > 2\phi_F$. The critical gate voltage, when there is formation of inversion layer at the surface , is called threshold voltage. Therefore, an n-type surface layer is formed not because of doping but due to inversion of originally p-type semiconductor due to large applied voltage. The inversion layer of electrons is separated from underlying p-type layer by depletion region. This formation of inversion layer is key to MOSFET operation.

Case - II : MOS Capacitor with n-type substrate

The biasing of a MOS capacitor with n-type semiconductor substrate for accumulation, depletion and inversion modes of operation is shown in Fig. 4.



(a) Accumulation mode (b) Depletion mode (c) Inversion mode

Fig.4 Biasing of MOS capacitor with n-type substrate (a) accumulatoin mode (b) depletion mode (c) inversion mode

Energy band diagram under equilibrium

Under idealized condition it is assumed that work function of metal is equal to the work function of semiconductor (i.e. $\phi_m = \phi_{sem}$) so that there is no difference in work functions. The Fermi level under idealized conditions at equilibrium when no bias is applied to the MOS capacitor is as shown in Fig.5(a). At equilibrium with zero bias the Fermi level on both sides of oxide layer is at the same level.

Energy band diagram under accumulation mode

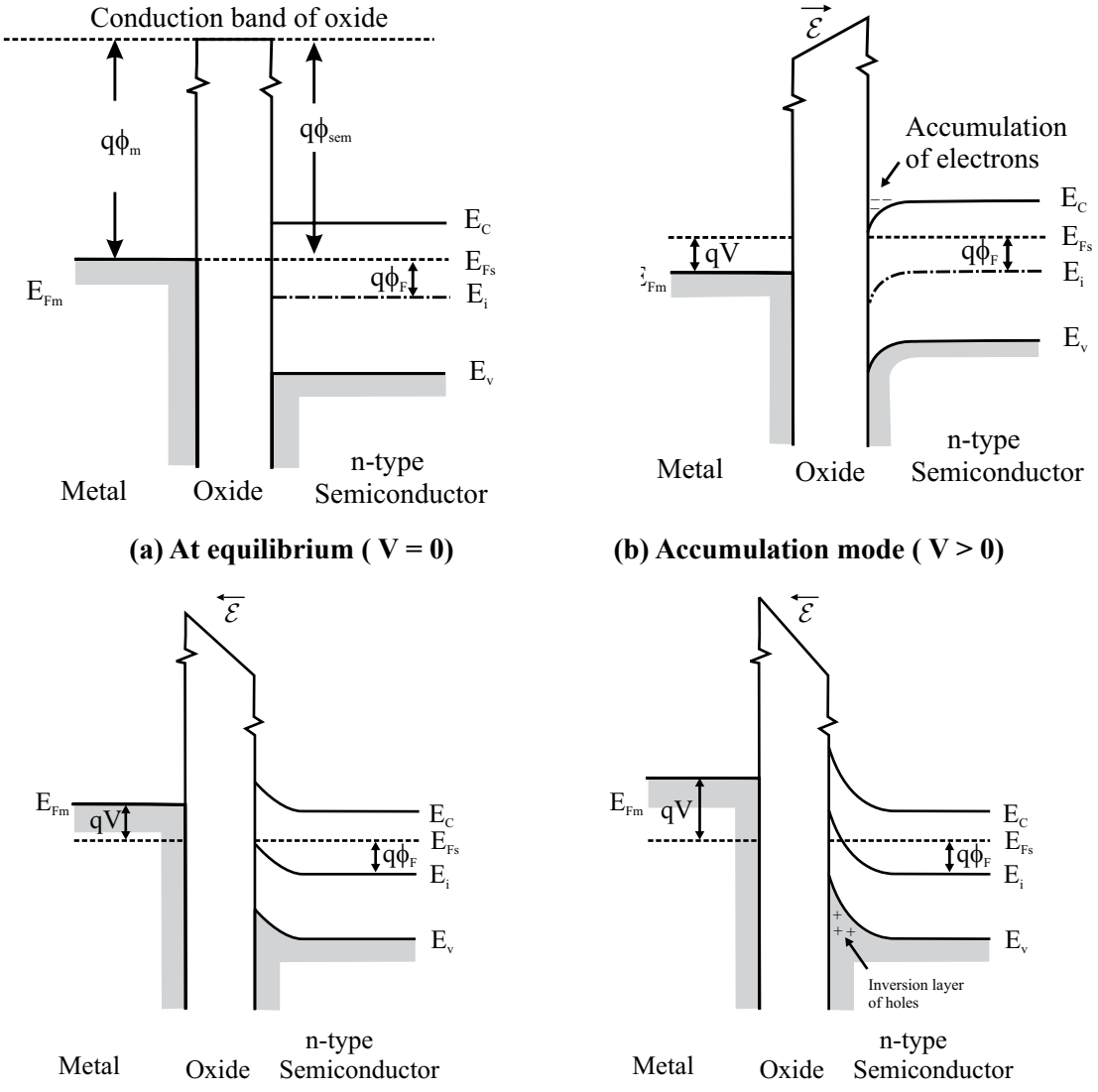
The MOS capacitor with n-type semiconductor substrate operates in accumulation mode when the metal gate is connected to positive terminal of the supply as shown inf Fig. 4(a). When gate terminal is connected to the positive potential gate metal acquires a positive charge. The positive charge on the gate metal induces an electric field ($\mathcal{E}$) in the oxide layer which in turn attracts electrons from the n-type semiconductor substrate and electrons are accumulated on the oxide-semiconductor interface as shown in the Fig. 5(b). The applied positive potential on gate terminal results in decrease in energy of electrons in metal. As a result Fermi level of metal, E_{Fm}, shifts below the equilibrium position (E_{Fs}) by qV, where V is applied voltage. The work function of metal ($q\phi_m$) and that of semi conductor ($q\phi_{sem}$) does not change with applied voltage so it results in tilting of conduction band of the oxide layer.

The accumulation of electrons at oxide-semiconductor interface results in increases in concentration of electrons at the interface. The increased concentration of electrons at the interface in semiconductor results in downward shifting of lowest level of conduction band (E_C) closer to the Fermi energy level (E_{Fs}) at the interface. Therefore, the lowest energy level of conduction band of semiconductor is tilted downward near the interface. Similar tilt is observed in intrinsic energy level(E_i) as well as highest energy level (E_V) of valence band of the semiconductor as shown in Fig. 5(b). The concentration of electrons in conduction of a semiconductor in terms of actual Fermi level and intrinsic Fermi level is given by,

$$n = n_i e^{(E_{Fs} - E_i)/kT} \quad (3)$$

It is observed from above equation that concentration of electrons near the oxide-semiconductor

interface can increase only if there is increase in difference $E_{Fs} - E_i$ near the interface. If there is no current in the semiconductor then there is no variation in Fermi level, E_{Fs}, in the semiconductor. So, the difference $E_{Fs} - E_i$ near the oxide-semiconductor interface is increased only by tilting the intrinsic level E_i downward at the interface. The Fermi level, E_{Fs}, at interface is more closer to the lower energy level of conduction band which means electrons concentration at interface is larger than that arising from the doping of n-type substrate.



(a) At equilibrium (V = 0) **(b) Accumulation mode (V > 0)**

(c) Depletion mode (V < 0) **(d) Inversion mode (V << 0)**

Fig.5 Energy band diagram of MOS with n-type semiconductor substrate (a) At thermal equilibrium (b) under accumulation mode (c) under depletion mode (d) under inversion mode

Energy band diagram under depletion mode

The MOS capacitor with n-type semiconductor substrate work in depletion mode when the

metal gate terminal of the capacitor is given a small negative potential as shown in Fig. 4(b). When gate terminal is connected to a small negative potential the gate metal acquires a negative charge. The applied negative potential on gate terminal results in increase in energy of electrons in gate metal. As a result Fermi level of metal E_{Fm} shifts upward from the equilibrium position (E_{Fs}) by qV. The negative charge on the gate metal induces an electric field ($\mathcal{E}$) in the oxide layer which repels the electrons away from oxide-semiconductor interface and, therefore, a depletion layer is formed below the gate region close to oxide-semiconductor interface as shown in Fig. 5(c). The depletion region near the interface consists of uncovered bound positive charges of donor impurity similar to the depletion region of pn junction. The depletion of electrons near the oxide-semiconductor interface results in decrease in concentration of electrons which in turn results in tilting of lowest energy level of conduction band (E_C) away from the Fermi level (E_{Fs}) near the interface in depletion region as shown in Fig. 5(c). Similar tilt is observed in intrinsic energy level as well as highest energy level of valence band of the semiconductor.

Energy band diagram under inversion mode

When negative potential of the metal gate is further increased there is a situation when intrinsic Fermi level E_i bends above the Fermi level E_{Fs} at oxide-semiconductor interface and the highest level of valence band (E_V) also bends upward and becomes closer to the Fermi level (E_{Fs}) as compared to lowest level of conduction band (E_C) as shown in Fig. 5(d). Therefore, the region near oxide-semiconductor interface has properties similar to that of a p-type semiconductor. This bending of E_i above E_{Es} at oxide-semiconductor result in large hole concentration in valence band near oxide-semiconductor interface. Therefore, a p-type surface layer is formed not because of doping but due to inversion of originally n-type semiconductor due to large applied voltage. The inversion layer of holes is separated from underlying n-type layer by depletion region.

4.2.2 Surface Potential, Carrier Concentration and Depletion Region Width in MOS Capacitor in Inversion Mode

Case - I : MOS Capacitor with p-type substrate

When MOS capacitor with a p-type substrate works in the inversion mode the intrinsic Fermi level(E_i) bends down below the Fermi level (E_{Fs}) at the oxide-semiconductor interface as shown in Fig. 6. Let $q\phi_F$ represents the difference in intrinsic Fermi level (E_i) and actual Fermi level (E_{Fs}) at equilibrium state in bulk of the semiconductor substrate and $q\phi_s$ represents bending of intrinsic Fermi level (E_i) at oxide-semiconductor interface. Let the energy level difference $q\phi$ represents extent of bends in energy band E_i from its equilibrium value at a distance x from the interface. Here ϕ_s is called surface potential which is a potential drop across the depletion layer of the capacitor. The condition $\phi_s = 0$ is known as flat band condition which is an ideal MOS. When $\phi_s < 0$ the energy band bends upward at the interface and there is hole accumulation and $\phi_s > 0$, there is formation of depletion region. When $\phi_s > 0$ and $q\phi_s > q\phi_F$ these is formation of inversion layer at the oxide-semiconductor interface. For strong inversion, the formation of n-type inversion layer should be as strong as p-type substrate. In other works there is condition called threshold of inversion when concentration of electrons at the

interface becomes concentration of holes in the bulk of substrate. This condition occurs when,

$$\phi_s = 2\phi_F \tag{4}$$

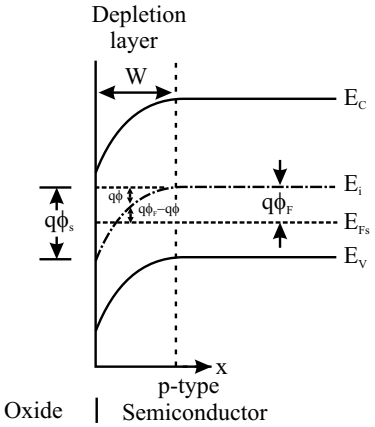


Fig.6 Energy band diagram of MOS with p-type semiconductor substrate under inversion mode

Expression of Surface Potential :

From the semiconductor theory it found that the concentration of holes in p-type substrate under thermal equilibrium state is given by,

$$p \approx N_A \approx N_V e^{-\frac{(E_{Fs}-E_V)}{kT}} \tag{5}$$

where N_V represents density of states in valence band and N_A is acceptor concentration.

Above equation can be further modified as under,

$$N_A = N_V e^{-\frac{(E_{Fs}-E_V-E_i+E_i)}{kT}} = N_V e^{-\frac{(E_i-E_V)}{kT}} e^{\frac{(E_i-E_{Fs})}{kT}} \tag{6}$$

$$\Rightarrow \quad N_A = n_i e^{\frac{(E_i-E_{Fs})}{kT}} \tag{7}$$

where, $n_i = N_V e^{-\frac{(E_i-E_V)}{kT}}$ = intrinsic carrier concentration (8)

From the energy band diagram of Fig.6, we have,

$$E_i - E_{Fs} = q\phi_F$$

$$\Rightarrow \quad N_A = n_i e^{\frac{q\phi_F}{kT}} \tag{9}$$

$$\Rightarrow \quad \boxed{\phi_F = \frac{kT}{q}\ell n\frac{N_A}{n_i} = V_T \ell n\frac{N_A}{n_i}} \tag{10}$$

where, $V_T = \frac{kT}{q}$ = Thermal voltage

The surface potential for at threshold inversion point,

$$\Rightarrow \quad \boxed{\phi_s = 2\phi_F = 2\frac{kT}{q}\ell n\frac{N_A}{n_i} = 2V_T\ell n\frac{N_A}{n_i}} \tag{11}$$

Carrier Concentrations on Interface :

The electron concentration in the p-type substrate region in bulk out of depletion region at thermal equilibrium is given by,

$$n_0 = \frac{n_i^2}{N_A} = \frac{n_i^2}{n_i e^{\frac{(E_i - E_{Fs})}{kT}}} = n_i e^{-\frac{(E_i - E_{Fs})}{kT}} \tag{12}$$

For bulk of p-type substrate away from depletion region, $E_i - E_{Fs} = q\phi_F$

$$\Rightarrow \quad n_o = n_i e^{-\frac{q\phi_F}{kT}} \tag{13}$$

For depletion region at any distance 'x' from oxide-semiconductor interface,

$$E_i - E_{Fs} = q\phi_F - q\phi$$

So, the electron concentration in depletion region at any distance from inerface is given by,

$$\Rightarrow \quad n = n_i e^{\frac{-q(\phi_F - \phi)}{kT}} = n_i e^{\frac{-q\phi_F}{kT}} \cdot e^{\frac{q\phi}{kT}} = n_o e^{\frac{q\phi}{kT}} \tag{14}$$

At the oxide-semiconductor interface, $\phi = \phi_s$. Therefore, the concentration of electrons at the interface (n_s),

$$\boxed{n_s = n_o e^{\frac{q\phi_s}{kT}}} \tag{15}$$

For strong inversion, $\phi_s = 2\phi_F$

$$\Rightarrow \quad \boxed{n_s = n_o e^{\frac{2q\phi_F}{kT}}} \tag{16}$$

Similarly, concentration of holes in the bulk region can be obtained using equation (7) as under,

$$p_0 = N_A = n_i e^{\frac{E_i - E_{Fs}}{kT}} = n_i e^{\frac{q\phi_F}{kT}} \tag{17}$$

For depletion layer region at distance 'x' from the interface, $E_i - E_{Fs} = q\phi_F - q\phi$

$$p = n_i e^{\frac{q(\phi_F - \phi)}{kT}} = n_i e^{\frac{q\phi_F}{kT}} \cdot e^{-\frac{q\phi}{kT}} = p_0 e^{-\frac{q\phi}{kT}} \tag{18}$$

Therefore, the concentration of holes at the interface (p_s), $\phi = \phi_s$

$$\therefore \quad \boxed{p_s = p_o e^{-\frac{q\phi_s}{kT}} = N_A e^{-\frac{q\phi_s}{kT}}} \tag{19}$$

For threshold inversion point, $\phi_s = 2\phi_F$

$$\Rightarrow \quad \boxed{p_s = N_A e^{-\frac{2q\phi_F}{kT}}} \tag{20}$$

Depletion Layer Width :

When a MOS capacitor works in inversion mode there is formation of depletion layer at oxide-semiconductor interface similar to a one side pn junction as shown in Fig.4.6. The space charge or depletion layer width in p-substrate near oxide-semiconductor interface is given similar to a one sided pn junction as under,

$$W = \sqrt{\frac{2\varepsilon_s \phi_s}{qN_A}} \tag{21}$$

Where $\varepsilon_s = \varepsilon_{rs}\varepsilon_o$, is permittivity of semiconductor, ε_{rs} is relative permitivity of semiconductor and ε_o is permititivy of free space. The surface potential ϕ_s is potential drop across the space charge region of the semiconductor substrate.

When surface potential $\phi_s = 2\phi_F$, the Fermi level at interface is above the intrinsic level where as it is below the intrinsic level in bulk of semiconductor. *The electron concentration at interface is same as hole concentration in bulk of semiconductor.* This condition is known as *threshold inversion point* and applied voltage across the MOS capacitor at threshold inversion point is known as *threshold voltage,* V_T. The sapce charge width at threshold inversion point is maximum. Beyond the threshold inversion point the electron concentration at the oxide-semiconductor interface increases exponentially with gate voltage but width of space charge or depletion layer does not change significantly. The maximum width of space charge is given by,

$$W_{max} = \sqrt{\frac{2\varepsilon_s \phi_s}{qN_A}} = \sqrt{\frac{4\varepsilon_s \phi_F}{qN_A}} \tag{22}$$

Putting expression of ϕ_F from equation (4.10) in above equation, we have,

$$\Rightarrow \quad W_{max} = \sqrt{\frac{4\varepsilon_s V_T}{qN_A} \ell n \frac{N_A}{n_i}} \tag{23}$$

Case - II : MOS Capacitor with n-type substrate

When MOS capacitor with a n-type substrate works in the inversion mode the intrinsic Fermi level(E_i) bends above the Fermi level (E_{Fs}) at the oxide-semiconductor interface as shown in Fig. 4.7.

Expression of Surface Potential :

From the semiconductor theory it found that the concentration of electrons in p-type substrate under

thermal equilibrium is given by,

$$n_o \approx N_D \approx N_C e^{-\frac{(E_C - E_{Fs})}{kT}} \tag{24}$$

where N_C represents density of states in conduction band and N_D is donor concentration. Above equation can be further modified as under,

$$N_D = N_C e^{-\frac{(E_C - E_{Fs} - E_i + E_i)}{kT}} = N_C e^{-\frac{(E_C - E_i)}{kT}} e^{\frac{(E_{Fs} - E_i)}{kT}} \tag{25}$$

$$\Rightarrow \quad N_D = n_i e^{\frac{(E_{Fs} - E_i)}{kT}} \tag{26}$$

where, $$n_i = N_C e^{-\frac{(E_C - E_i)}{kT}} = \text{intrinsic carrier concentration} \tag{27}$$

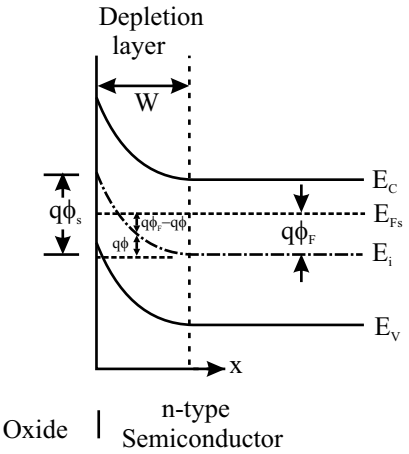


Fig.7 Energy band diagram of MOS with p-type semiconductor Substrate under inversion mode

From the energy band diagram shown above, we have,

$$E_{Fs} - E_i = q\phi_F$$

$$\Rightarrow \quad N_D = n_i e^{\frac{q\phi_F}{kT}} \tag{28}$$

$$\Rightarrow \quad \boxed{\phi_F = \frac{kT}{q} \ell n \frac{N_D}{n_i} = V_T \ell n \frac{N_D}{n_i}} \tag{29}$$

The surface potential for strong inversion,

$$\Rightarrow \quad \boxed{\phi_s = 2\phi_F = 2\frac{kT}{q} \ell n \frac{N_D}{n_i} = 2V_T \ell n \frac{N_D}{n_i}} \tag{30}$$

Carrier Concentrations on Interface :

The hole concentration in the n-type substrate at thermal equilibrium in given by,

$$p_o = \frac{n_i^2}{N_D} = \frac{n_i^2}{n_i e^{\frac{(E_{Fs}-E_i)}{kT}}} = n_i e^{-\frac{(E_{Fs}-E_i)}{kT}} \quad (31)$$

For bulk of p-type substrate away from depletion region, $E_i - E_{Fs} = q\phi_F$

$$\Rightarrow \quad p_o = n_i e^{-\frac{q\phi_F}{kT}} \quad (32)$$

For depletion region at any distance 'x' from oxide-semiconductor interface,

$$E_i - E_{Fs} = q\phi_F - q\phi$$

Then hole concentration at any distance 'x' from oxide-semiconductor interface can be written as under,

$$p = n_i e^{\frac{-q(\phi_F-\phi)}{kT}} = n_i e^{\frac{-q\phi_F}{kT}} \cdot e^{\frac{q\phi}{kT}} = p_o e^{\frac{q\phi}{kT}} \quad (33)$$

At the oxide-semiconductor interface, $\phi = \phi_s$. Therefore, the concentration of holes at the interface (p_s),

$$\boxed{p_s = p_o e^{\frac{q\phi_s}{kT}}} \quad (34)$$

For strong inversion, $\phi_s = 2\phi_F$

$$\Rightarrow \quad \boxed{p_s = p_o e^{\frac{2q\phi_F}{kT}}} \quad (35)$$

Similarly, concentration of electrons can be obtained using equation (28) as under,

$$n_o = N_D = n_i e^{\frac{E_{Fs}-E_i}{kT}} = n_i e^{\frac{q\phi_F}{kT}} \quad (36)$$

The concentration of electrons at distance 'x' from the interface,

and $$n = n_i e^{\frac{q(\phi_F-\phi)}{kT}} = n_i e^{\frac{q\phi_F}{kT}} \cdot e^{-\frac{q\phi}{kT}} = n_0 e^{-\frac{q\phi}{kT}} \quad (37)$$

Therefore, the concentration of electrons at the interface (n_s),

$$\boxed{n_s = n_o e^{-\frac{q\phi_s}{kT}} = N_D e^{-\frac{q\phi_s}{kT}}} \quad (38)$$

For strong inversion, $\phi_s = 2\phi_F$

$$\Rightarrow \quad \boxed{n_s = n_o e^{-\frac{2q\phi_F}{kT}} = N_D e^{-\frac{2q\phi_F}{kT}}} \quad (39)$$

Depletion Layer Thickness :

The space charge or depletion layer width in n-substrate near oxide-semiconductor interface is given similar to a one sided pn junction as under,

$$W = \sqrt{\frac{2\varepsilon_s \phi_s}{qN_D}} \tag{40}$$

The depletion layer width is maximum at threshold inversion point with $\phi_s = 2\phi_F$. So, the maximum width of depletion layer in n-type substrate is given by,

$$W_{max} = \sqrt{\frac{2\varepsilon_s \phi_s}{qN_D}} = \sqrt{\frac{4\varepsilon_s \phi_F}{qN_D}} \tag{41}$$

Putting expression of ϕ_F from equation (4.29) in above equation, we have,

$$\Rightarrow \quad W_{max} = \sqrt{\frac{4\varepsilon_s V_T}{qN_D} \ell n \frac{N_D}{n_i}} \tag{41a}$$

4.2.3 Charge Distribution, Electric Field and Electric Potential in MOS capacitor

The charge density, electric field and electric potential in a MOS capacitor with p-type substrate working in strong inversion mode of operation with gate voltage more than a limiting value called threshold voltage is shown in Fig.8.

Charge Distribution

In inversion mode of operation, the depletion region of MOS capacitor with p-substrate consists of negative charge of inversion layer at the interface and uncovered negative charge of acceptor impurity atoms. The width of inversion is of order of 100 $\mathring{A}$ which is negligible as compared to total width of depletion layer. The charge density in depletion layer due to uncovered impurity ions at threshold inversion point,

$$Q_d = -q N_A W \tag{42}$$

Let Q_{inv} is charge density of inversion layer of electrons at oxide-semiconductor interface. The inversion charge density is taken into account only when gate voltage is more than a limiting voltage called threshold voltage. Then total charge density (Q_s) on substrate side of the capacitor is given by,

$$Q_s = Q_d + Q_{inv} = -qN_A W + Q_{inv} \tag{43}$$

The total positive charge on gate metal plate is equal to net negative charge in semiconductor in the depletion region to maintain charge neutrality.

$$Q_m = -Q_s = -(Q_d + Q_{inv}) = qN_A W - Q_{inv} \tag{44}$$

$$\Rightarrow \quad \boxed{Q_m = qN_A W - Q_{inv}} \tag{45}$$

Here, Q_m, Q_d, Q_{inv} and Q_s are charge densities whose value will be negative for negative ions or electrons and positive for holes or positive ions.

The charge per unit area of depletion region at threshold of inversion is given by

$$Q_{dT} = -q\,N_A\,W_{max} \tag{46}$$

Putting the expression of W_{max} from equation (4.23) in above equation, we have,

$$\Rightarrow \quad Q_{dT} = -q\,N_A\sqrt{\frac{4\varepsilon_s V_T \ell n\frac{N_A}{n_i}}{q\,N_A}} = -\sqrt{4qN_A\varepsilon_s\,V_T\,\ell n\frac{N_A}{n_i}} \tag{47}$$

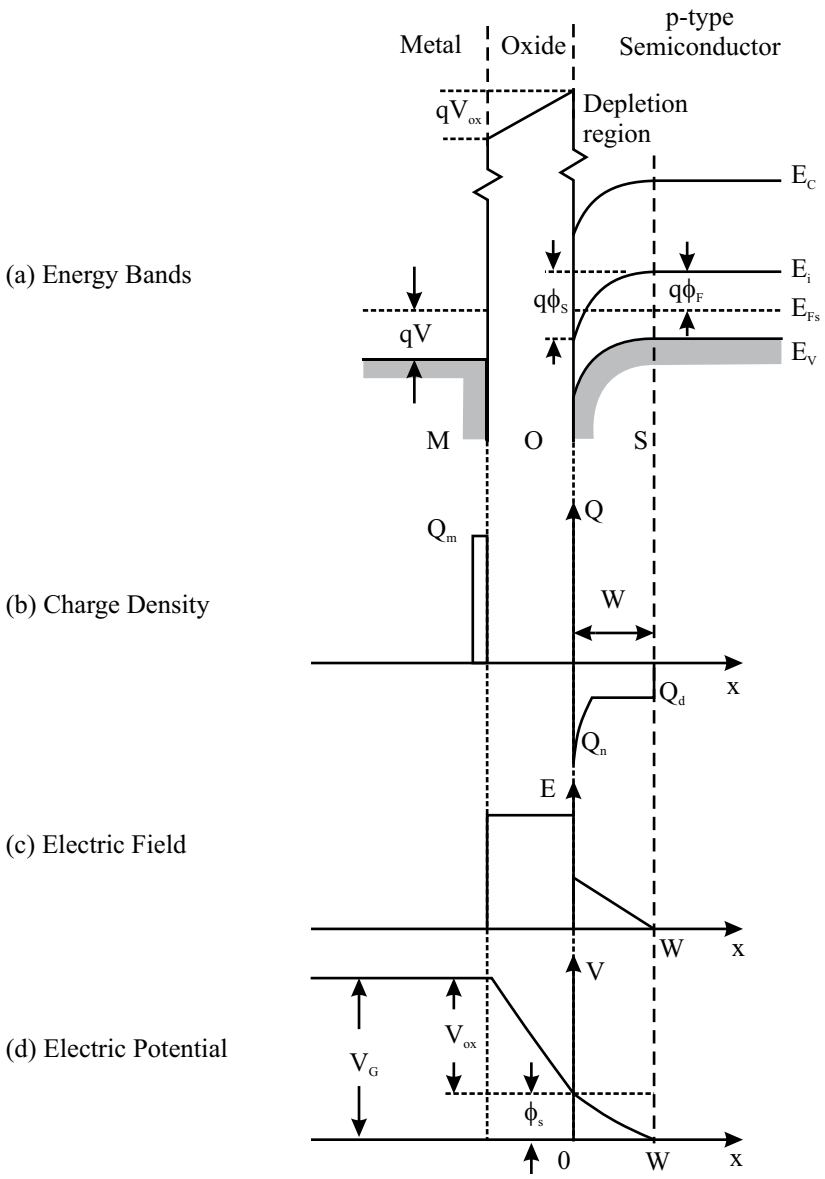


Fig.8 Energy band diagram , charge density, electric field and electric potential of MOS capacitor with p-type substrate in inversion mode of operation.

Electric Potential

Under the ideal conditions with equal value of work function of gate metal and semiconductor, the applied voltage at the gate of MOS capacitor appears partially across oxide layer and partially across the depletion layer as under,

$$V_G = V_{ox} + \phi_s \tag{48}$$

The potential difference across oxide layer is related to the capacitance of oxide layer as under,

$$V_{ox} = \frac{Q_m}{C_{ox}} = -\frac{Q_s}{C_{ox}} \tag{49}$$

where Q_m is surface charge density at metal- oxide interface, Q_s is surface charge density at oxide-semiconductor interface and C_{ox} is capacitance per unit area of the oxide layer.

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{50}$$

where ε_{ox} is primitivity of oxide layer and t_{ox} is thickness of oxide layer.

$$\Rightarrow \quad V_{ox} = -\frac{Q_s}{\varepsilon_{ox}} t_{ox} \tag{51}$$

Note: *The surface potential is considered to be positive when energy bands bend downward and it is negative when energy bands bend upward.*

Electric Field ($\mathcal{E}$) :

The electric filed in the depletion region in semiconductor near the oxide-semiconductor interface varies linearly in manner similar to depletion region of one sided pn junction. The maximum electric field intensity at oxide-semiconductor interface due to acceptor ions in depletion layer is given by,

$$\mathcal{E}_{d,max} = \frac{}{\varepsilon_s} = -\frac{qN\ W}{\varepsilon_s} \tag{53}$$

Putting expression of W from equation (21) in above equation, we have,

$$\mathcal{E}_{d,max} = \frac{qN_A}{\varepsilon_s}\sqrt{\frac{2\varepsilon_s\phi_s}{qN_A}} \tag{54}$$

$$\Rightarrow \quad \mathcal{E}_{d,max} = \sqrt{\frac{2qN_A\phi_s}{\varepsilon_s}} \tag{55}$$

Modifying above equation ,we have,

$$\Rightarrow \quad \mathcal{E}_{d,max} = \sqrt{\frac{4\phi_s^{\ 2}}{(2\varepsilon_s\phi_s / qN_A)}} \tag{56}$$

$$\Rightarrow \quad \mathcal{E}_{d,max} = \frac{2\phi_s}{W} \tag{57}$$

For threshold inversion point, $W = W_{max}$, $\phi_s = 2\phi_F$

$$\therefore \quad \mathcal{E}_{dT} = \frac{4\phi_F}{W_{max}} \tag{58}$$

Electric field at Strong Inversion :

When MOS capacitor works in strong inversion mode there is formation of inversion layers of charges carriers at oxide-semiconductor interface. Total charge in substrate in inversion mode is given by equation (43). Electric intensity at oxide-semiconductor interface in substrate can be given as,

$$\mathcal{E}_{inv} = \frac{Q_s}{\varepsilon_s} = \frac{Q_{dT} + Q_{inv}}{\varepsilon_s} \tag{59}$$

Total electric field at the oxide-semiconductor interface at threshold inversion point on semiconductor side,

$$\mathcal{E}_s = \mathcal{E}_{dT} + \mathcal{E}_{inv} \tag{60}$$

$$\Rightarrow \quad \mathcal{E}_s = \frac{Q_{dT}}{\varepsilon_s} + \frac{Q_{inv}}{\varepsilon_s} \tag{61}$$

$$\Rightarrow \quad \mathcal{E}_s = -\frac{qN_A W_{max}}{\varepsilon_s} + \frac{Q_{inv}}{\varepsilon_s} = \frac{4\phi_F}{W} + \frac{Q_{inv}}{\varepsilon_s} \tag{62}$$

According to boundary conditions at oxide-semiconductor interface, the charge densities must be same at the interface on both sides of the interface.

So, $$|Q_m| = |Q_s| \tag{63}$$

$$\boxed{\varepsilon_{ox}\mathcal{E}_{ox} = \varepsilon_s\mathcal{E}_s} \tag{64}$$

Where ε_s is permittivity of semiconductor and $\mathcal{E}$ is electric field intensity in semiconductor at the interface.

Example 1

An ideal MOS capacitor has boron doping-concentration fo 10^{15} cm^{-3} in the substrate. When a gate voltage is applied, a depletion region of width 0.5 μm is formed with a surface (channel) potential of 0.2 V. Given that $\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm and the relative permittivities of silicon and silicon dioxide are 12 and 4, respectively, the peak electric field (in V/μm) in the oxide region is_____

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Solution : Ans : 2.3 to 2.5

The boron is an acceptor or p-type impurity. If doping impurity is Baron then semiconductor is p-type.

Given, acceptor concentration, $N_A = 10^{15}$ cm^{-3}

Depletion region width, $W = 0.5\ \mu m$

Surface potential, $\phi_s = 0.2\ V$

Relative permittivity of Si, $\varepsilon_{rs} = 12$

Relative permittivity of oxide, $\varepsilon_{rox} = 4$

$$\varepsilon_o = 0.854 \times 10^{-14}\ F/cm$$

If there is formation of depletion region, the MOS capacitor must be working on depletion mode with positive gate voltage. The charge stored in depletion layer per unit area is given by,

$$Q_d = qNA\,W$$

$$\Rightarrow \quad Q_d = 1.6\times10^{-19}\times10^{15}\times0.5\times10^{-4}$$

The maximum electric field on oxide semiconductor interface is given by,

$$E_s = \frac{Q_d}{\varepsilon_{rs}\varepsilon_o} = \frac{qN_A W}{\varepsilon_s} \qquad \text{....(i)}$$

Where, $\varepsilon_s = \varepsilon_{rs}\varepsilon_o$

Width of depletion layer in MOS capacitor is given by,

$$W = \sqrt{\frac{2\varepsilon_s}{q}\frac{1}{N_A}\cdot\phi_s}$$

Putting expression of W in equation (i), we have,

$$E_s = \frac{qN_A}{\varepsilon_s}\sqrt{\frac{2\varepsilon_s}{q}\cdot\frac{1}{N_A}\cdot\phi_s} = \sqrt{\frac{2q}{\varepsilon_s}\cdot N_A\cdot\phi_s}$$

$$\Rightarrow \quad E_s = \sqrt{\frac{4.\phi_s^2}{\frac{2\varepsilon}{q}\cdot\frac{1}{N_A}\cdot\phi_s}} = \frac{2\phi_s}{W}$$

$$\Rightarrow \quad E_s = \frac{2\times0.2}{0.5\times10^{-6}} = 0.8\times10^6$$

According boundary condition of electric field at oxide-semiconductor interface,

$$\varepsilon_s E_s = \varepsilon_{ox} E_{ox}$$

$$\Rightarrow \quad E_{ox} = \frac{\varepsilon_s}{\varepsilon_{ox}}\cdot E_s = \frac{12}{4}\times0.8\times10^6 = 2.4\times10^6\ V/m = 2.4\ V/\mu m$$

4.2.4 Variation of surface charge density as a function of surface potential

The variation of surface charge density in a MOS capacitor with p-type substrate is shown in Fig.9

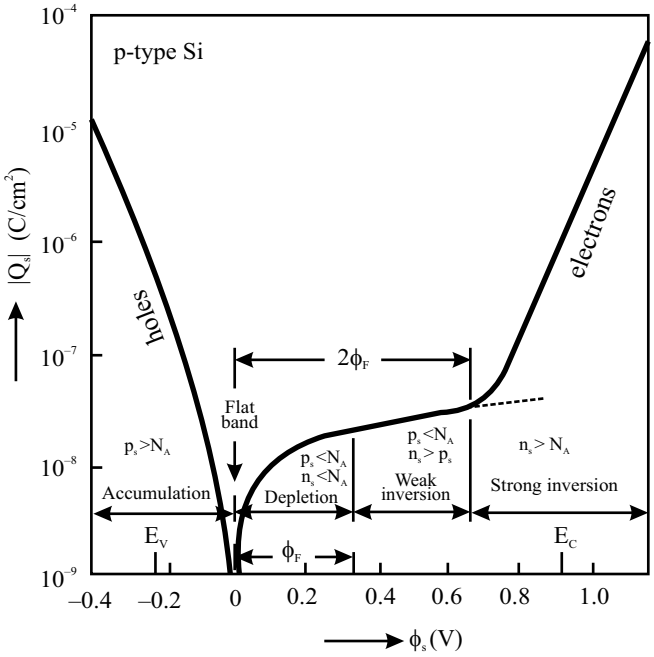


Fig.9 Variation of surface charge density in accumulation, depletion and inversion modes as a function of surface potential

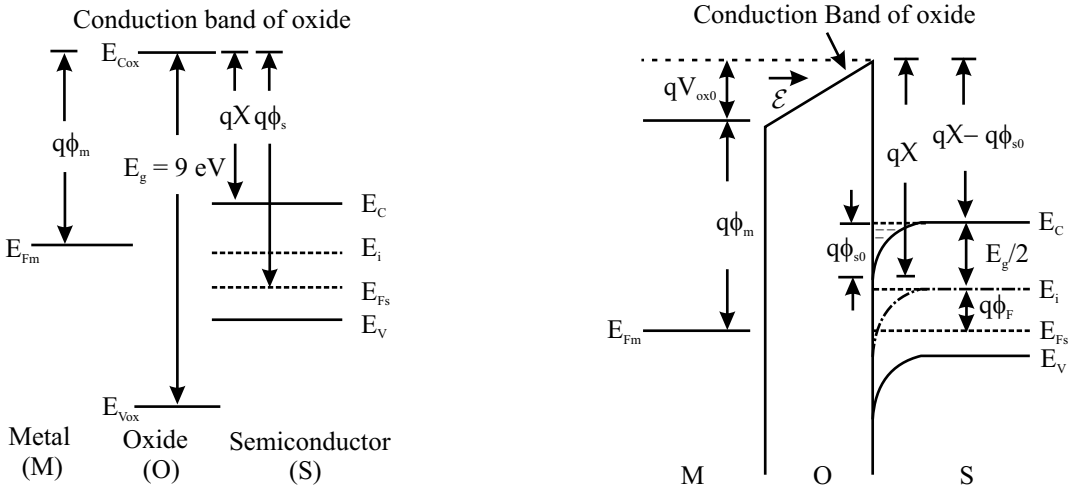
It observed from above figure that

1. Under flat band condition i.e. $\phi_s = 0$ the net space charge is zero. This is because fixed dopant charges are canceled by mobile carrier charges at flat band.
2. When surface potential is negative it attracts and forms an accumulation layer of majority carrier holes at the interface. The concentration of holes at surface (p_s) is more than the acceptor impurity concentration (N_A).
3. The device works in depletion mode for a positive surface potential in the range, $0 < \phi_s < \phi_F$, In depletion mode both concentration of holes (p_s) and electrons (n_s) at interface is less than the acceptor concentration.
4. For $\phi_F < \phi_s < 2\phi_F$, the Fermi energy ($E_F$) at surface is in upper half at surface which implies an n-type material, but have not yet reached at threshold inversion point. This condition is referred as weak inversion. In weak inversion concentration of electrons is more than concentration of holes at interface but it is less than the acceptor concentration.
5. When $\phi_s > 2\phi_F$, the electron density on surface increases rapidly with increase in surface potential resulting in strong inversion. In strong inversion mode the concentration of electrons at interface is more than the acceptor concentration in bulk and behaviour becomes like n-type material at interface.

4.2.5 Work Function Difference

For MOS devices the work function of metal ($q\phi_m$) is taken as energy required to move an electron from the Fermi level of metal (E_{Fm}) to the conduction band of oxide (E_{Cox}) and work function of semiconductor ($q\phi_s$) is defined as the energy required to move an electron from Fermi level of semiconductor (E_{Fs}) to conduction band of oxide. The energy required to move an electron from conduction band of semiconductor (E_C) to conduction band of oxide is called electron affinity (qX) of the semiconductor. The location of Fermi level in a semiconductor depends on doping level of

the semiconductor. Therefore, the work function of semiconductor depends on doping level of the semiconductor and it may not be same as the work function of the metal. In this case the work function of semiconductor is assumed to be greater than that of the metal. The energy band diagram of metal, oxide and semiconductors before making the contact is shown in Fig. 10(a). When metal-oxide-semiconductor contact is made, the Fermi energy level of metal shifts downward to align with Fermil level of semiconductor at thermal equilibrium as shown in Fig. 10(b). Since the work functions of metal and semiconductor remain unaltered during this process, therefore, there is downward bending of conduction band of the oxide on metal-oxide interface. Bending of conduction band of oxide layer under thermal equilibrium induces an electric field ($\mathcal{E}_o$) in the oxide layer with higher potential on semiconductor side as compared to metal side. The potential difference across the oxide layer is V_{ox0} at thermal equilibrium with zero bias voltage applied across the MOS capacitor. The induced electric field in the oxide layer repels holes away from interface of oxide-semiconductor interface and thus a depletion layer is formed near the interface. This depletion layer has uncovered negative bound charges of acceptor impurities. Thus a surface potential (ϕ_{s0}), similar to built in potential of a depletion layer of pn junction, is developed across the depletion layer formed on semiconductor side of oxide-semiconductor interface. The reduction of concentration of holes near the interface results in bending of valence band downward, away from the Fermi level (E_F), at the interface to accommodate reduction in concentration of holes. Similar bend is observed in intrinsic Fermi level (E_i) and conduction band (E_C) of the semiconductor. Bending of conduction band (E_C) at the interface also increases the electron affinity(qX) at the interface. Fig.10 shows the energy band diagram of MOS capacitor with p-type substrate at thermal equilibrium before making contact and after making contact with zero bias voltage applied.



(a) Before making contact **(b) After making contact**

Fig.10 Energy band diagram of MOS capacitor with p-type substrate at thermal equilibrium (a) before making contact (b) after making contact with zero bias voltage

As Fermi levels on both side of the oxide layer is at the same level, therefore, we have,

$$q\phi_m + qV_{ox0} = (qX - q\phi_{s0}) + \frac{E_g}{2} + q\phi_F \qquad (65)$$

$$\Rightarrow \quad V_{ox0} + \phi_{s0} = -\left[\phi_m - \left(X + \frac{E_g}{2q} + \phi_F\right)\right] \tag{66}$$

$$\Rightarrow \quad V_{ox0} + \phi_{s0} = -\phi_{ms}$$

where,
$$\phi_{ms} = \phi_m - \left(X + \frac{E_g}{2q} + \phi_F\right) \tag{67}$$

$$\Rightarrow \quad \phi_{ms} = \phi_m - \phi_s \tag{68}$$

where,
$$\phi_s = X + \frac{E_g}{2q} + \phi_F = \text{work function of semiconductor} \tag{69}$$

The potential ϕ_{ms} is known as metal semiconductor work function difference.

Similarly metal-semiconductor work function difference for a MOS-capacitor with n-type substrate can be given by

$$\phi_{ms} = \phi_m - \phi_s = \phi_m - \left(X + \frac{E_g}{2q} - \phi_F\right) \tag{70}$$

Note : i. For MOS capacitor with p-substrate, the work function (ϕ_s) of semiconductor is more than work function (ϕ_m) of metal there work function difference (ϕ_{ms}) is negative for MOS capacitor with p-substrate.

ii. For MOS capacitor with n-substrate , the work function (φs) of semiconductor is less than work function (ϕ_m) of metal there work function difference (ϕ_{ms}) is positive for MOS capacitor with n-substrate.

4.2.6 Flat Band Voltage

It is observed from previous section that there exists a work function difference (ϕ_{ms}) in a MOS capacitor at thermal equilibrium due to difference in work functions of semiconductor and gate metal. It results in shifting of Fermi level in metal as well as bending of energy bands at oxide-semiconductor interface. An external gate voltage called *Flat Band Voltage* is required to be applied at which there is no bending of energy bands at the metal-semiconductor interface and there is zero net charge is space charge region as shown in Fig.11.

Case-I : When there is no trapped charge in oxide layer

If a gate voltage V_G is applied, the potential drop across the oxide and surface potential will change which can be given as,

$$V_G = \Delta V_{ox} + \Delta\phi_s = (V_{ox} - V_{oxo}) + (\phi_s - \phi_{so}) \tag{71}$$

$$\Rightarrow \quad V_G = V_{ox} + \phi_s + \phi_{ms} \tag{72}$$

Where, V_{ox} is voltage drop across oxide layer and ϕ_s is surface potential.

At flat band there is no bending of energy bands at the metal-semiconductor interface so the surface potential is zero at flat band condition.

$$\therefore \quad \phi_s = 0 \tag{73}$$

The space charge in depletion layer is also zero at flat band condition so the voltage drop across the

oxide layer is zero at flat band.

$$\therefore \quad V_{ox} = 0 \tag{74}$$

The flat band voltage is obtained by putting $\phi_s = 0$ and $V_{ox} = 0$ in equation (72),

i.e. $$V_{FB} = \phi_{ms} = \phi_m - \phi_s \tag{75}$$

Putting this relation in equation (4.72), we have,

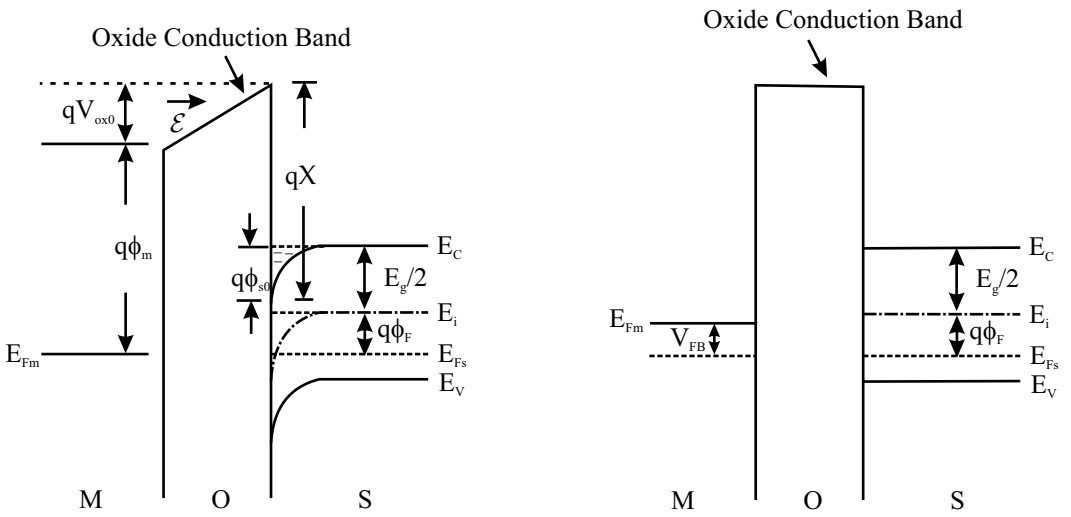
$$V_G = V_{ox} + \phi_s + V_{FB} \tag{76}$$

For the MOS capacitor with p-substrate, the work function (ϕ_s) of semiconductor is more than work function (ϕ_m) of metal, therefore, flat band voltage is negative for MOS capacitor with p-substrate.

Similarly, for the MOS capacitor with n-substrate, the work function (ϕ_s) of semiconductor is less than work function (ϕ_m) of metal, therefore, flat band voltage is negative for MOS capacitor with p-substrate.

Case-II : Considering work function difference as well as trapped charges of oxide layer

The oxide layer always contains the trapped positive charges due to imperfection in the oxide (SiO_2) layer. If the effect of positive trapped charges in oxide layer is also taken into account then the flat band voltage is required will be function of work function difference and density of trapped positive charge in the oxide layer. The trapped positive charge normally appears close to oxide-semiconductor interface.



(a) At thermal equilibrium (b) At flat band

Fig. 11 Energy band diagram of MOS capacitor at (a) At thermal equilibrium (b) At flat band

Let equivalent trapped charge per unit area located in oxide near oxide-semiconductor interface is Q_x. The metal-semiconductor work function difference for a zero bias gate voltage is given by

$$-\phi_{ms} = V_{oxo} + \phi_{so} \tag{77}$$

If no biasing voltage is applied then there is no charge in the semiconductor. The trapped oxide charges in the oxide layer induces charges on the metal-oxide interface such that,

$$Q_m + Q_x = 0 \quad (78)$$

$$\Rightarrow \quad Q_m = -Q_x \quad (79)$$

The charge distribution due to trapped charges on oxide layer with zero bias voltage applied to the MOS capacitor is shown in Fig. 12.

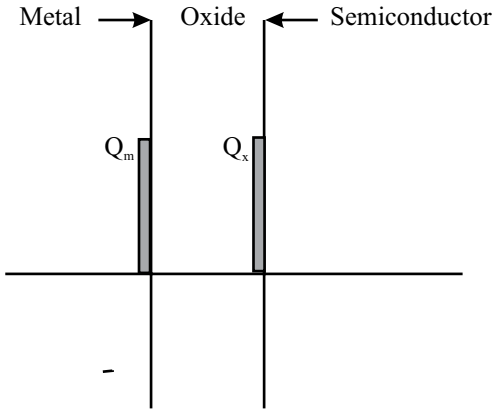


Fig.12 Charge distribution in MOS capacitor at flat band

The voltage across the oxide layer is given by,

$$V_{ox} = \frac{Q_m}{C_{ox}} \quad (80)$$

$$\Rightarrow \quad V_{ox} = -\frac{Q_x}{C_{ox}} \quad (81)$$

In flat band condition oxide-semiconductor surface potential is zero as $\phi_s = 0$. Then gate voltage V_G given by equation (4.49) become a flat band voltage,V_{FB} as under,

$$\therefore \quad \boxed{V_{FB} = V_{ox} + \phi_{mx} = -\frac{Q_x}{C_{ox}} + \phi_{mx}} \quad (82)$$

Example 2

A MOS capacitor is fabricated on p-type Si (silicon) where the metal work function is 4.1 eV and electron affinity of Si is 4.0 eV. E_C–F_F = 0.9 eV, where E_C and E_F are the conduction band minimum and the Fermi energy levels of Si, respectively. Oxide $\varepsilon_r = 3.9$, $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm, oxide thickness $t_{ox} = 0.1\mu m$ and electronic charge q = 1.6 × 10–19 C. If the measured flat band voltage of the capacitor is –1V, then the magnitude of the fixed charge at the oxide-semiconductor interface, in nC/cm², is _____.

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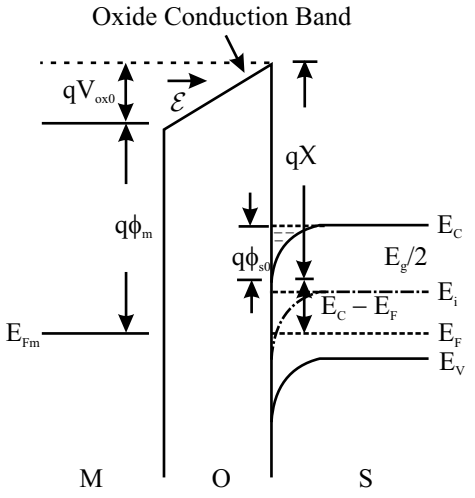
Solution : Ans. : 6.85 to 6.95

Given, $q\phi_m = 4.1$ eV

$$\Rightarrow \quad \phi_m = \frac{4.1eV}{q} = \frac{4.1eV}{1.6\times10^{-19}} = 4.1V$$



Electron affinity of Si, $qX = 4.0$ eV

$$\Rightarrow \quad X = \frac{4.0\text{eV}}{q} = \frac{4.0\text{eV}}{1.6\times10^{-19}} = 4.0\text{V}$$

Difference of energy levels,

$$E_C - F_F = 0.9 \text{ eV}$$

$$\frac{E_C - E_F}{q} = \frac{0.9\text{eV}}{q} = \frac{0.9\text{eV}}{1.6\times10^{-19}} = 0.9\text{V}$$

Using above figure the work function difference of MOS capacitor is given by,

$$q\phi_{ms} = q\phi_m - (qX + E_C - F_F)$$

$$\Rightarrow \quad \phi_{ms} = \phi_m - \left(X + \frac{E_C - E_F}{q}\right)$$

$$\Rightarrow \quad \phi_{ms} = 4.1 - (4.0 + 0.9) = -0.8 \text{ V}$$

The flat band voltage with fixed trapped charge in oxide layer is given by,

$$V_{FB} = \phi_{ms} - \frac{Q_x}{C_{ox}}$$

$$\Rightarrow \quad V_{FB} = \phi_{ms} - \frac{Q_x}{\varepsilon_{rox}\varepsilon_o} t_{ox}$$

From the given data,

$\varepsilon_{rox} = 0.9$, $\varepsilon_0 = 8.85 \times 10^{14}$ F/cm, $t_{ox} = 0.1\ \mu m = 0.1 \times 10^{-4}$ c.m., $V_{FB} = -1V$

$$\Rightarrow \quad -1 = -0.8 - \frac{Q_x}{\varepsilon_{rox}\varepsilon_o}.t_{ox}$$

$$\Rightarrow \quad Q_x = \frac{0.2 \times 3.9 \times 8.85 \times 10^{-14}}{0.1 \times 10^{-4}} = 6.903 \text{ nC/cm}^2$$

4.2.7 Threshold Voltage

The threshold voltage is applied gate voltage at which threshold inversion point occurs in semiconductor near the oxide-semiconductor interface of the MOS capacitor. In MOS capacitor, the threshold inversion point occurs when surface potential, $\phi_s = 2\phi_F$. The width of depletion layer in semiconductor region is maximum at threshold inversion point. Fig.13 shows the charge distribution in MOS capacitor at threshold inversion point for a p-type semiconductor substrate.

At the threshold inversion point the depletion layer width near oxide-semiconductor interface in semiconductor is maximum. If Q_x is trapped positive charge density in oxide, Q_{mT} is positive charge density per unit area metal gate at threshold inversion point. The sum of all the charges in metal, oxide and substrate must be zero to maintain electrical neutrality.

$$Q_x + Q_{mT} + Q_{sT} = 0 \tag{83}$$

$$\Rightarrow \quad Q_{mT} = -Q_{sT} - Q_x \tag{84}$$

The maximum space charge per unit area at oxide-semiconductor interface is given by,

$$Q_{sT} = Q_{dT} = -q N_A W_{max} \tag{85}$$

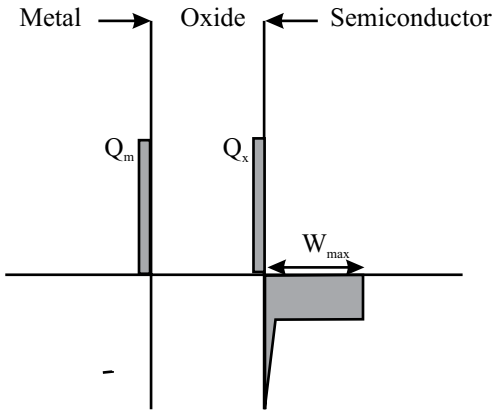


Fig.13 Charge distribution in MOS capacitor with p-substrate threshold inversion point

The applied gate voltage is given in terms of surface potential as,

$$V_G = V_{ox} + \phi_s + \phi_{ms} \tag{86}$$

At threshold inversion point, $\phi_s = 2\phi_F$ and gate voltage is equal to the threshold voltage creating electrons inversion layer of charge at oxide-semiconductor interface.

$$\boxed{V_T = V_{oxT} + 2\phi_F + \phi_{ms}} \tag{87}$$

Where V_{oxT} is voltage across the oxide at the threshold inversion point. The energy band diagram of MOS capacitor with p-substrate and an applied positive gate voltage, V_G under threshold inversion point is as shown in Fig.14.

The voltage across oxide layer at threshold inversion point can be given by,

$$V_{oxT} = \frac{Q_{mT}}{C_{ox}} = -\frac{Q_{sT} + Q_x}{C_{ox}} = -\frac{Q_{dT} + Q_x}{C_{ox}} \quad (88)$$

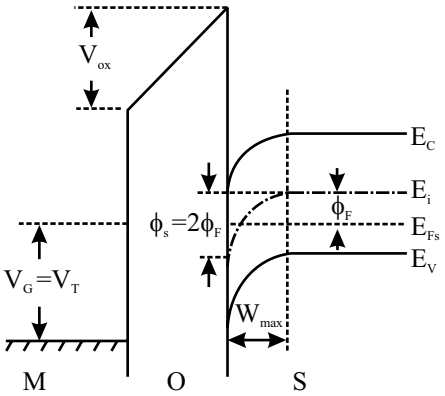


Fig.14 Energy band diagram of MOS capacitor with p-substrate at threshold inversion point

Then threshold voltage becomes as under,

$$V_T = -\frac{Q_{dT} + Q_x}{C_{ox}} + \phi_{ms} + 2\phi_F \quad (89)$$

$$\Rightarrow \quad V_T = -\frac{Q_{dT}}{C_{ox}} - \frac{Q_x}{C_{ox}} + \phi_{ms} + 2\phi_F \quad (90)$$

$$\Rightarrow \quad V_T = -\frac{Q_{dT}}{C_{ox}} + 2\phi_F + V_{FB} \quad (91)$$

Where, $V_{FB} = -\frac{Q_x}{C_{ox}} + \phi_{mx}$ = flat band voltage.

The charge density at interface at threshold inversion point is given by,

$$Q_{sT} = Q_{dT} = -q\, N_A\, W_{max} \quad (92)$$

$$\Rightarrow \quad \boxed{V_T = \frac{qN_A W_{max}}{C_{ox}} + 2\phi_F + V_{FB}} \quad (93)$$

4.2.8 Gate Voltage at Strong Inversion

There is condition of strong inversion in a MOS capacitor when the gate voltage becomes more than the threshold voltage. The width of depletion layer is fixed at W_{max} at strong inversion and charge density of depletion layer is same as its threshold value. There is additional charge density on oxide-semiconductor interface due to inversion layer. The surface potential across the depletion is also fixed at $\phi_s = 2\phi_F$ at strong inversion. Therefore, if gate voltage is increased beyond threshold voltage

then additional voltage drops across the oxide layer only.

For strong inversion the charge of substrate,

$$Q_s = Q_{dT} + Q_{inv} \tag{94}$$

If trapped positive charge in oxide layer is also considered then equivalent charge on metal gate,

$$Q_m = -(Q_s + Q_x) = -Q_{dT} - Q_{inv} - Q_x \tag{95}$$

The voltage drop across the oxide layer,

$$V_{ox} = \frac{Q_m}{C_{ox}} = -\frac{Q_{dT} + Q_{inv} + Q_x}{C_{ox}} \tag{96}$$

From equation (86), the gate voltage is given by,

$$V_G = V_{ox} + \phi_s + \phi_{ms}$$

$$\Rightarrow \quad V_G = -\frac{Q_{dT} + Q_{inv} + Q_x}{C_{ox}} + \phi_{ms} + \phi_s \tag{97}$$

$$\Rightarrow \quad V_G = -\frac{Q_{inv}}{C_{ox}} - \frac{Q_{dT}}{C_{ox}} + 2\phi_F - \frac{Q_x}{C_{ox}} + \phi_{ms} \tag{98}$$

Putting expression of flat band voltage from equation (81) in above equation, we have,

$$\Rightarrow \quad V_G = -\frac{Q_{inv}}{C_{ox}} - \frac{Q_{dT}}{C_{ox}} + \phi_s + V_{FB} \tag{99}$$

For strong inversion region of operation, $\phi_s = 2\phi_F$

$$\Rightarrow \quad V_G = -\frac{Q_{inv}}{C_{ox}} - \frac{Q_{dT}}{C_{ox}} + 2\phi_F + V_{FB} \tag{100}$$

Putting expression of threshold voltage from equation (91) in above equation, we have,

$$\Rightarrow \quad \boxed{V_G = -\frac{Q_{inv}}{C_{ox}} + V_T} \tag{101}$$

where,

$$\boxed{V_T = -\frac{Q_{dT}}{C_{ox}} + 2\phi_F + V_{FB}} \tag{102}$$

The charge density of inversion layer can be obtained from equation (101), as under,

$$\boxed{Q_{inv} = -C_{ox}(V_G - V_T)} \tag{103}$$

Example 3

A voltage V_G is applied across a MOS capacitor with metal gate and p-type silicon substrate at T = 300 K. The inversion carrier density (in number of carriers per unit area) for $V_G = 0.8$ V is 2×10^{11} cm^{-2} For $V_G =$ 1.3 V, the inversion carrier density is 4×10^{11} cm^{-2}. What is the value of the inversion carrier density for $V_G = 1.8$ V?

(a) 4.5×10^{11} cm^{-2} (b) 6.0×10^{11} cm^{-2}

(c) 7.2×10^{11} cm^{-2} (d) 8.4×10^{11} cm^{-2}

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Solution : Ans. (b)

Given, $T = 300$ K

The inversion carrier density of MOS capacitor with p-substrate in terms of gate voltage is given by

$$Q_{inv} = -C_{ox}(V_G - V_T)$$

where C_{ox} is capacitance per unit area of oxide and V_T is threshold voltage.

Given charge is not mentioned to be negative that means it must be magnitude of the charge. So, taking only magnitude, we have,

$$Q_{inv} = C_{ox}(V_G - V_T) \quad .....(i)$$

Case-I $Q_{inv} = 2 \times 10^{11}$ cm^{-2}

when $V_G = 0.8$ V

$$\Rightarrow \quad 2 \times 10^{11} = C_{ox}(0.8 - V_T)$$

$$\Rightarrow \quad C_{ox} = \frac{2 \times 10^{11}}{0.8 - V_T} \quad ....(ii)$$

Case-II $Q_{inv} = 4 \times 10^{11}$ cm^{-2}

when $V_G = 1.3$V.

$$\Rightarrow \quad 4 \times 10^{11} = C_{ox}(1.3 - V_T)$$

$$\Rightarrow \quad C_{ox} = \frac{4 \times 10^{11}}{1.3 - V_T} \quad ....(iii)$$

From (i) and (ii), we have,

$$\frac{2 \times 10^{11}}{0.8 - V_T} = \frac{4 \times 10^{11}}{1.3 - V_T}$$

$$\Rightarrow \quad 1.3 - V_T = 1.6 - 2V_T$$

$$\Rightarrow \quad V_T = 0.3\text{V}$$

Putting value of V_T in equation (ii), we have,

$$C_{ox} = \frac{2 \times 10^{11}}{0.8 - 0.3} = 4 \times 10^{11} \text{ F/cm}^2$$

When $V_G = 1.8$ V the inversion charge density can be obtained values of C_{ox} and V_T in equation (i) as under,

$$Q_{inv} = 4 \times 10^{11} (1.8 - 0.3) \text{ cm}^{-2}$$

$$\Rightarrow \quad Q_{inv} = 6.0 \times 10^{11} \text{ cm}^{-2}$$

4.2.9 Capacitance-Voltage Characteristics of MOS Capacitor

The capacitance of MOS device is function of applied voltage and it is given by,

$$C = \frac{dQ}{dV}$$

Under ideal condition it is assumed that there is no charge trapped in oxide as will as in oxide-semiconductor interface. There are three operating conditions in MOS capacitor which are accumulation, depletion and inversion.

Case-I : Ideal condition

A. Accumulation Mode

In accumulation mode of operation of MOS capacitor the metal gate is given negative potential which induces accumulation layer of holes in the substrate at the oxide-semiconductor interface. The capacitance per unit area of MOS capacitor for accumulation mode is oxide capacitance which is given by,

$$\boxed{C_{(acc.)} = C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}} \quad (104)$$

The charge distribution in accumulation mode of a MOS capacitor with p-substrate is as shown in Fig.15.

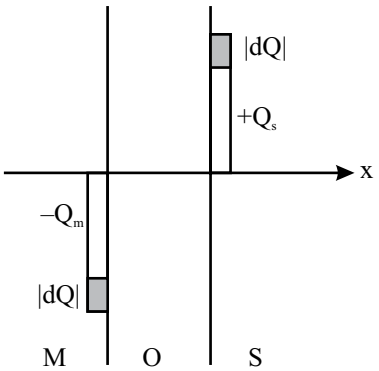


Fig.15 Charge distribution in MOS capacitor with p-substrate in accumulation mode

B. Depletion Mode

A MOS capacitor with p-type substrate works in depletion mode when metal gate is connected to small positive voltage. The applied small positive potential induces a space charge region in substrate near oxide-semiconductor interface. The metal acquires a positive charge due to applied positive voltage and depletion region near interface contains the negative bound charges of acceptor impurity. The charge distribution in depletion mode of a MOS capacitor with p-substrate is as shown in Fig.16.

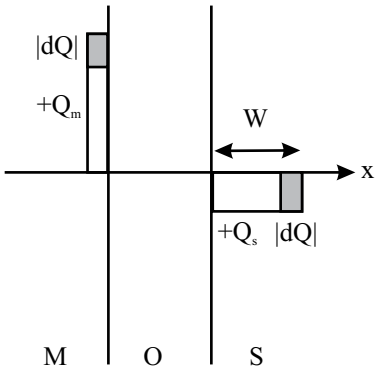


Fig.16 Charge distribution in MOS capacitor with p-substrate in depletion mode

In depletion mode, the MOS capacitor offers two capacitances appearing in series. One capacitance is due to oxide layer and second capacitance is due to formation of depletion layer in semiconductor near oxide-semiconductor interface. The capacitance of oxide layer is fixed where as capacitance of depletion layer is function of applied bias voltage. The total capacitance per unit area in depletion mode is given by,

$$\boxed{C_{(dep)} = \frac{C_{ox}\, C_d}{C_{ox} + C_d}} \tag{105}$$

where C_d is capacitance per unit are of depletion region.

The capacitance per unit are of depletion region is given by,

$$\boxed{C_d = \frac{\varepsilon_s}{W}} \tag{106}$$

Where ε_s is permittivity of semiconductor and W is width of depletion layer.

$$\therefore \quad C_{(dep)} = \frac{C_{ox}}{1 + \frac{C_{ox}}{C_d}} = \frac{\varepsilon_{ox} / t_{ox}}{1 + \frac{\varepsilon_{ox}}{t_{ox}} \cdot \frac{W}{\varepsilon_s}} \tag{107}$$

$$\Rightarrow \quad C_{(dep)} = \frac{\varepsilon_{os}}{1 + \frac{\varepsilon_{ox}}{\varepsilon_s} \cdot W} \tag{108}$$

The capacitance $C_{(dep)}$ decreases with increase in width of depletion layer. The width of depletion is maximum at Threshold of inversion point threshold gate voltage. Therefore, capacitance offered by MOS capacitor is minimum at threshold inversion point. The minimum capacitor of MOS capacitor can be given by,

$$\therefore \quad C'_{min} = \frac{\varepsilon_{ox}}{t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_s} \cdot W_{max}} \tag{109}$$

Where, $$W_{max} = \sqrt{\frac{4\varepsilon_s}{q} \cdot \frac{1}{N_A} \cdot \phi_{Fp}} = \sqrt{\frac{4\varepsilon_s}{q} \cdot \frac{1}{N_A} \cdot V_T \ell n \frac{N_A}{n_i}} \tag{110}$$

C. Inversion mode

In inversion mode of operation, it is the charge of inversion layer and gate metal which varies with applied gate voltage. When gate voltage becomes more than the threshold value the width of depletion layer becomes maximum and thus the charge in depletion region does not change when gate voltage is increased above threshold value. Fig. 17 shows the charge distribution of MOS capacitor with p-substrate in inversion mode.

The capacitance offered by MOS capacitor in inversion mode is oxide capacitance which is given by

$$C_{(inv)} = C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{111}$$

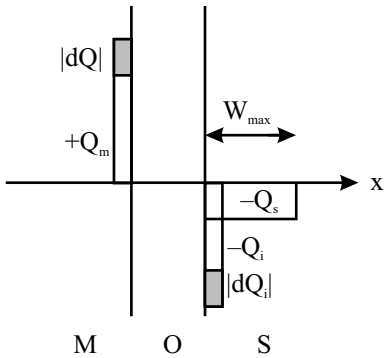


Fig.17 Charge distribution in MOS capacitor with p-substrate in inversion mode

The variation in capacitance of MOS of a MOS capacitor as a function of gate voltage is shown in Fig. variate min MOS capacitance w.r.t. gate voltage is shown in Fig.18

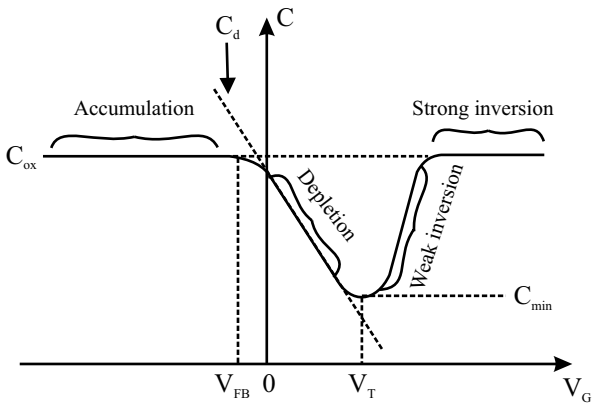


Fig.18 Variation in MOS capacitance with gate voltage

Case-II : Effect of frequency

In an inversion mode of MOS capacitor with p-type substrate, there is formation of inversion layer of electrons at oxide-semiconductor interface. The inversion layer of electron is formed due to diffusion of electrons from p-substrate across the depletion layer and due to thermal generation of electron-hole pairs within the space charge region. If MOS capacitor is subjected to an a.c. voltage the concentration of electrons in inversion layer cannot change instantaneously. In such case capacitor-

voltage (C-V) characteristics of MOS capacitor is function of frequency of the ac signal. At very high frequency the charge of inversion fails to respond to change in gate voltage. At high frequencies the differential change in charge occurs with gate voltage due to change of space charge width. The capacitance of MOS capacitor is at its minimum value at high frequency as shown in Fig.19.

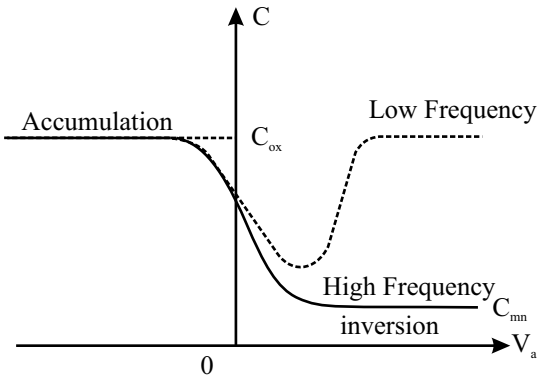


Fig.19 Variation in MOS capacitance with frequency

High frequency in above figure corresponds to 10 MHz and low frequency corresponds to it 10 kHz.

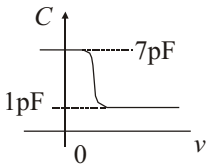
Case-III. Effect of oxide trapped charges

A MOS capacitor can have fixed trapped positive charge in oxide layer. The flat band voltage becomes more negative and threshold voltage reduces due to positive trapped charge in the oxide layer of a MOS capacitor with p-type substrate.

Example 4

Common Data for Question A & B :

The figure shows the high-frequency capacitance-voltage (C-V) characteristics of a Metal/SiO_2 / silicon (MOS) capacitor having an area of 1×10^{-4} cm^2. Assume that the permitivities $(\varepsilon_0\varepsilon_r)$ of silicon and SiO_2 are 1×10^{-12} F/cm and 3.5×10^{-13} F/cm respectively.



A. The gate oxide thickness in the MOS capacitor is

(a) 50nm (b) 143nm

(c) 350 nm (d) 1 μm

GATE(EC/2007/2M)

B. The maximum depletion layer width in silicon is

(a) 0.143 μm (b) 0.857 μm

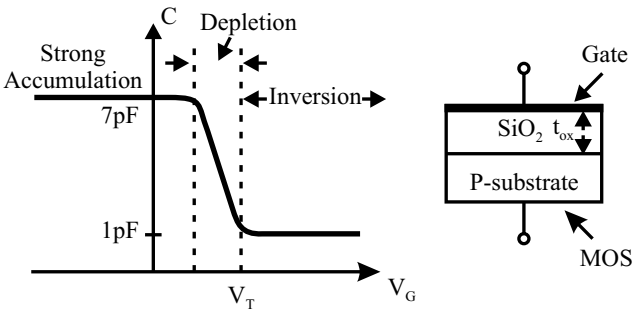
(c) 1 μm (d) 1.143 μm

GATE(EC/2007/2M)

Solution:

A. Ans.(a)

The C-V characteristics of MOS capacitor at frequency operation are shown below,



When gate voltage is negative there is accumulation of holes below oxide layer in MOS capacitor with p-substrate.

In such case oxide layer only offers a capacitance which is given by,

$$C_i = \frac{\varepsilon_{ox} A}{t_{ox}} \qquad \text{.....(i)}$$

where,

ε_{ox} → Permitivity of oxide layer

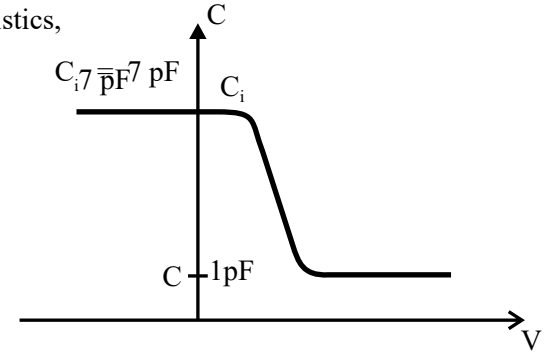
A → Area of gate electrode or area of capacitor

t_{ox} → Thickness of oxide

Given, $\varepsilon_{ox} = 3.5 \times 10^{-13}$ F/cm

$A = 1 \times 10^{-4}$ cm^{-2}

From given characteristics,



Putting above values in equation (i), we have,

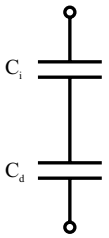
$$7 \times 10^{-12} = \frac{3.5 \times 10^{-13} \times 1 \times 10^{-4}}{t_{ox}}$$

$$\Rightarrow \quad t_{ox} = \frac{3.5 \times 10^{-17}}{7 \times 10^{-12}} = \frac{1}{2} \times 10^{-5} \text{ cm}$$

$\Rightarrow \quad t_{ox} = 50 \text{ nm}$

B. Ans.(b)

When voltage is more than threshold voltage the capacitance of MOS capacitor is minimum. When gate voltage applied is positive a depletion layer is also formed in p-substrate below oxide layer. This depletion layer also offers a capacitance. Both oxide layer and depletion layer capacitances applies in series. The equivalent capacitance of combination is given as,



$$C = \frac{C_i C_d}{C_i + C_d}$$

Where, $C_d = \frac{\varepsilon_s}{W}$ = Depletion layer capacitor

W = Width of depletion layer

ε_s = Permittvity of Si

Beyond V_T, C_d is minimum and W is maximum.

$$\therefore \quad C = \frac{C_i C_{d\,min}}{C_i + C_{d\,min}} \qquad .....(ii)$$

$$\therefore \quad C_{d\,min} = \frac{\varepsilon_s A}{W_{max}} \qquad ....(iii)$$

From given characteristics,

$$C = 1 \text{ pF} \;\&\; C_i = 7 \text{ pF}$$

$$\therefore \quad 1 = \frac{7 \times C_{d,min}}{7 + C_{d,min}}$$

$$\Rightarrow \quad 7 + C_{d\,min} = 7\, C_{d\,min}$$

$$\Rightarrow \quad C_{d\,min} = \frac{7}{6} \text{ pF}$$

Putting $C_{d,\,min}$ in equation (iii), we have,

$$\frac{7}{6} \times 10^{-12} = \frac{\varepsilon_s A}{W_{max}}$$

Given, $\varepsilon_s = 1\times10^{-12}$ F/cm

$A = 1 \times 10^{-4}$ cm^{-2}

$$\Rightarrow \quad \frac{7}{6}\times10^{-12} = \frac{1\times10^{-12}\times1\times10^{-4}}{W_{max}}$$

$$\Rightarrow \quad W_{max} = \frac{6}{7}\times10^{-4}\text{cm}$$

$$\Rightarrow \quad W_{max} = 0.857\ \mu\text{m}$$

Example 5

In a MOS capacitor with an oxide layer thickness of 10 nm, the maximum depletion layer thickness is 100 nm. The permittivities of the semiconductor and the oxide layer are ε_s and ε_{OX} respectively. Assuming $\frac{\varepsilon_s}{\varepsilon_{OX}} = 3$, the ratio of the maximum capacitance to the minimum capacitance of this MOS capacitor is .....

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Solution : Ans.(4.3 to 4.4)

Given thickness of oxide layer,

$$t_{ox} = 10 \text{ nm}$$

Maximum thickness of depletion layer,

$$W_{max} = 100 \text{ nm}$$

Ratios of permittivity of semiconductor to oxide,

$$\frac{\varepsilon_s}{\varepsilon_{ox}} = 3$$

The maximum capacitance of MOS capacitor is equal to capacitance of oxide layer which is given by,

$$C_{max} = C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \qquad .....(i)$$

The minimum capacitance of MOS capacitor is observed when depletion layer thickness is maximum. The minimum capacitance of MOS capacitor is equal to series combination of capacitance of oxide layer and lowest capacitance of depletion layer.

$$\therefore \quad C_{min} = \frac{C_{ox}C_{d,min}}{C_{ox}+C_{dmin}} \qquad .....(ii)$$

where, $C_{dmin} = \frac{\varepsilon_s}{W_{max}}$

From (i) and (ii), we have,

$$\frac{C_{max}}{C_{min}} = \frac{C_{ox}+C_{d\,min}}{C_{d\,min}} = 1+\frac{C_{ox}}{C_{d\,min}}$$

$$\Rightarrow \quad \frac{C_{max}}{C_{min}} = 1+\frac{\varepsilon_{ox}}{t_{ox}}\cdot\frac{W_{max}}{\varepsilon_s}$$

$$\Rightarrow \quad \frac{C_{max}}{C_{min}} = 1+\frac{1}{3}\times\frac{100\times10^{-9}}{10\times10^{-9}} = 4.33$$

4.3 Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs)

MOS Field Effect Transistor (MOSFET) has become most popular device due to it design on integrated circuits fabricated on single Silicon chip. It is also known as Insulated Gate Field Effect Transistor (IGFET).

4.3.1 Physical Structure and Symbols of MOSFET

A MOSFET has four terminals called Source (S), Drain (D), Gate (G) and Body (B). The body terminal (B) is normally shorted with the source terminal. So, only source, drain and gate terminals will be discussed in the following section. MOSFET has a conducting channel between source and drain to provide path for the drain current. The source is the terminal at which majority carriers enter into the channel and drain is the terminal at which the majority carriers leave the channel. The gate is control terminal of MOSFET. The potential of gate terminal controls the drain current of MOSFET. Therefore, MOSFET is a voltage controlled device and it can be used as a voltage controlled current source. The construction of MOSFET is symmetrical so the functions of source and drain can be interchanged in a MOSFET. The gate terminal is separated from body of MOSFET by an oxide layer which acts as an insulating layer. The

Types of MOSFET

i) Enhancement type: (a) n-channel (b) p-channel.

ii) Depletion type: (a) n-channel (b) p-channel.

Enhancement type n-channel MOSFET

An enhancement type n-channel MOSFET consists of p-type substrate on single Si wafer in which two n^+ layers are diffused to act as source and drain. A thin layer of oxide (SiO_2) is grown on the surface of substrate between drain and source regions. The layer of oxide act as an insulator between gate and body of MOSFET. A thin layer of metal is deposited on oxide layer to act as a gate electrode of the MOSFET. Metallic contacts are also made with source, drain and body for external connections of the MOSFET. An n-channel MOSFET is alternatively known as NMOS transistor.

Fig.20 shows the physical structure and symbols of a n-channel enhancement type MOSFET.

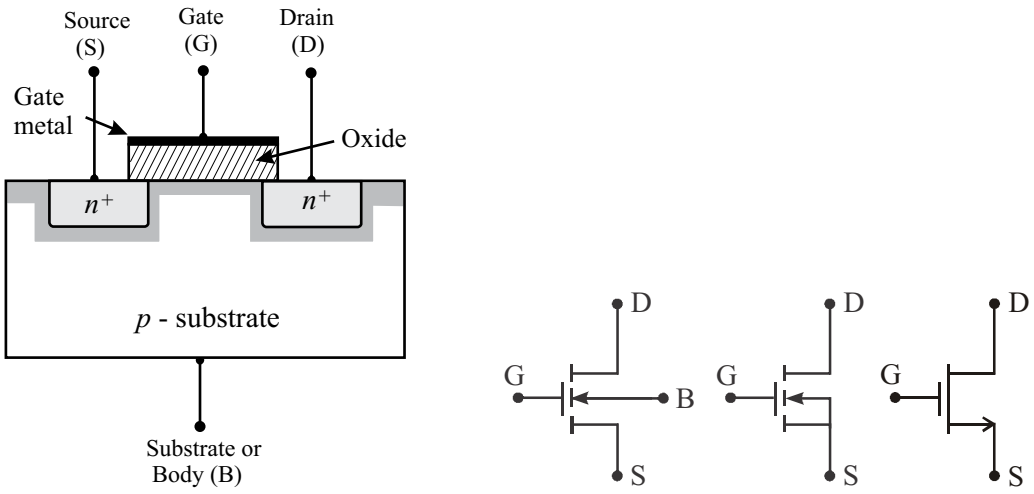


Fig. 20 Physical structure and symbols of enhancement type n-channel MOSFET

Enhancement type p-channel MOSFET

The physical structure of an enhancement type p-channel MOSFET is similar to that of enhancement type n-channel MOSFET. The only difference is that the substrate is n-type material and p^+ layers form source and drain of the MOSFET. A p-channel MOSFET is alternatively known as PMOS transistor. Fig. 21 shows the physical structure and symbols of enhancement type p-channel MOSFET.

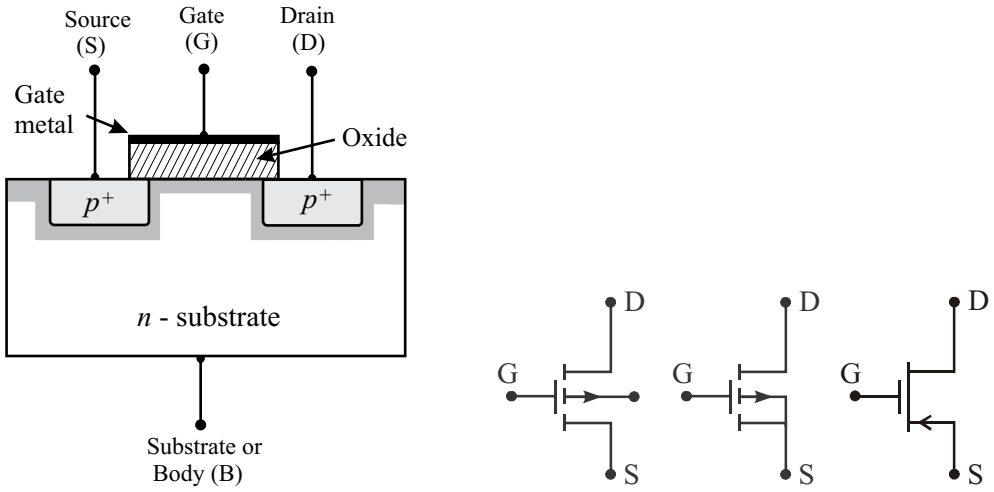


Fig. 21 Physical structure and symbols of enhancement type p-channel MOSFET

Depletion type n-channel MOSFET

The physical structure of a depletion type n-channel MOSFET is similar to n-channel enhancement type MOSFET except that it has a thin n-type layer below the oxide layer which forms a conducting

channel between source and drain regions. Fig.22 shows the physical structure and symbols of a depletion type n-channel MOSFET.

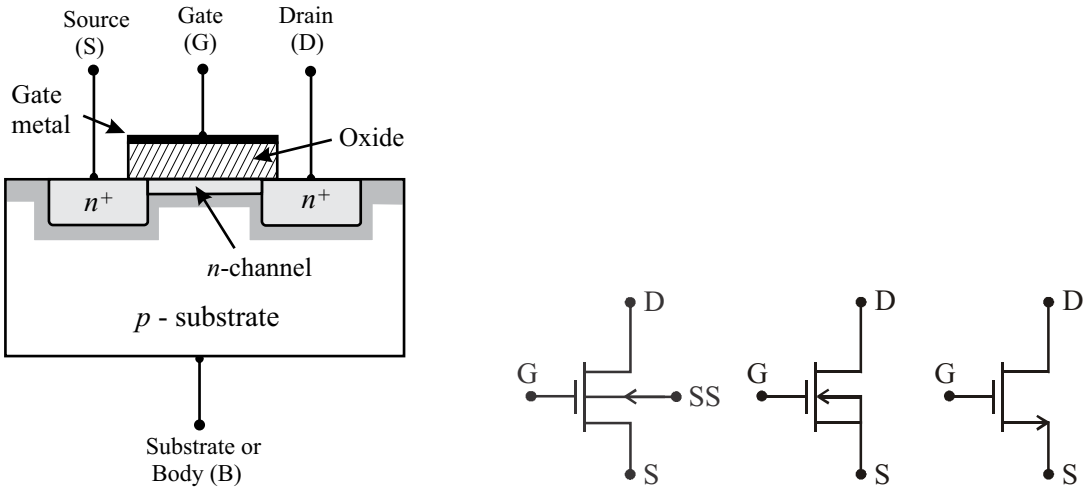


Fig. 22 Physical structure and symbols of depletion type n-channel MOSFET

Depletion type p-channel MOSFET

The physical structure of a depletion type p-channel MOSFET is similar to p-channel enhancement type MOSFET except that it has a thin p-type layer below the oxide layer which forms a conducting channel between source and drain regions. Fig.23 shows the physical structure and symbols of a depletion type p-channel MOSFET.

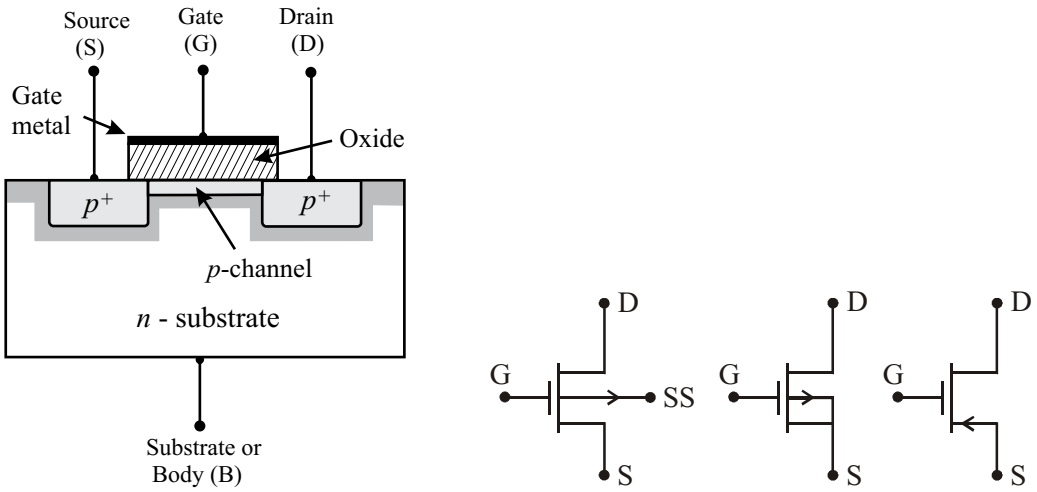


Fig. 23 Physical structure and symbols of depletion type p-channel MOSFET

4.3.2 Operation of MOSFET

Case-I: Operation of Enhancement type MOSFET

The n-channel enhancement type MOSFET is most commonly used transistor among all the

MOSFETs. Enhancement type n-channel MOSFET is a MOS capacitor with two n^+ regions diffused in the p-type substrate. When the gate terminal is connected to a positive potential, it forms a depletion layer below the oxide-semiconductor interface between source and drain regions. Fig.24 shows the biasing arrangement of an enhancement type n-channel MOSFET. If gate voltage (V_G) is increased, there is accumulation of electrons at the oxide-semiconductor interface.

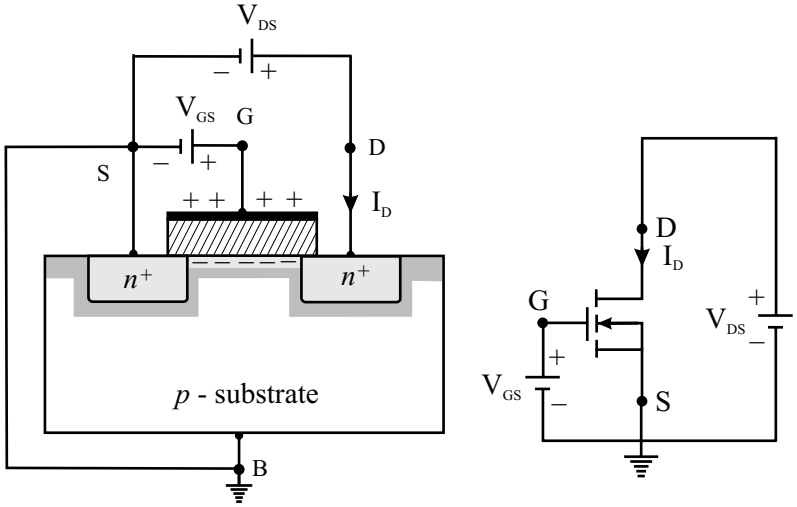


Fig. 24 Operation of enhancement type n-channel MOSFET with positive voltage at gate and n-channel between drain and source regions.

If gate voltage becomes equal to a value called threshold voltage (V_T) then sufficient number of electrons are accumulated in the region below oxide layer between source and drain regions forming a conducting channel of inversion layer. This channel provides a path for current flow from drain to source due to drain to source voltage. In a MOSFET, the source is the terminal at which majority carriers enter into the channel and drain is the terminal at which majority carriers leave the channel. In n-channel MOSFET, the electrons are majority carriers so the electrons must enter at source and leave at drain, therefore, negative terminal of battery is connected at the source and positive terminal is connected to the drain and drain current flows from drain to source. Reverse is true for a p-channel enhancement type of MOSFET. Since, the drain current is due to majority carriers only, therefore, MOSFET is an example of unipolar device.

Note: *The operation of enhancement type p-channel MOSFET is similar to that of enhancement type n-channel MOSFET. In p-channel MOSFET the conducting channel is formed by holes accumulated below the oxide-semiconductor interface between drain and source regions. The voltages V_{GS}, V_{DS} and drain current I_D are negative in case of a p-channel MOSFET.*

Case-II: Operation of depletion type MOSFET

The depletion type n-channel MOSFET , the electrons in n-layer diffused between source and drain regions form a conducting channel. Fig.24a shows the biasing arrangement of a depletion type n-channel MOSFET. When the gate terminal is connected to a negative potential, it forms a depletion layer below the oxide-semiconductor interface between source and drain. If negative bias voltage (V_G) at gate is increased, the width of depletion layer in the channel increases and effective width of the conducting channel formed by n-layer decreases and hence the channel resistance increases and

drain current decreases. Since, the drain current decreases with increase in biasing voltage at gate terminal therefore, this MOSFET is known as depletion type of MOSFET. A depletion type MOSFET has non-zero current when gate voltage is zero. The bias voltage at gate terminal of depletion type n-channel MOSFET can be positive or negative. The drain current increases with increase positive voltage applied at gate and it decreases with increase in negative bias voltage applied at gate. Therefore, the depletion type MOSFET can work in depletion as well as enhancement modes of operation.

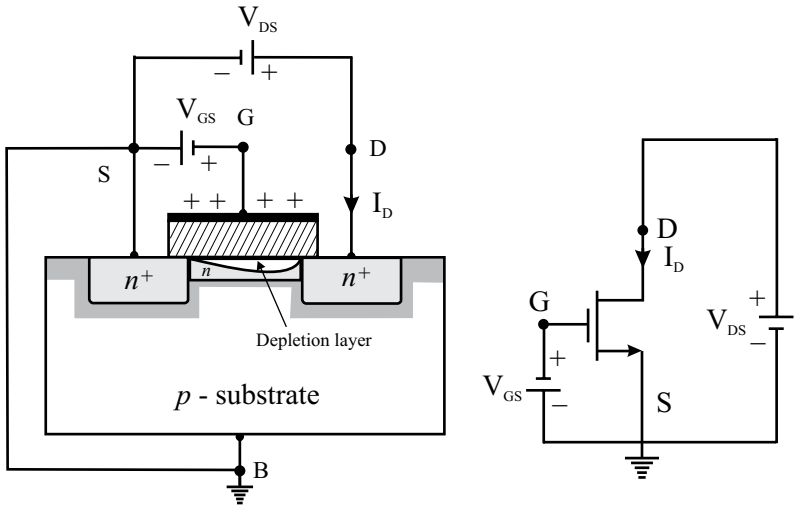


Fig. 24a Operation of depletion type n-channel MOSFET with negative voltage at gate and positive voltage between drain and source regions.

Note: *The operation of depletion type p-channel MOSFET is similar to that of depletion type n-channel MOSFET. In depletion type p-channel MOSFET, the conducting channel is formed by holes in p-layer diffused between drain and source regions. The voltages V_{GS}, V_{DS} and drain current I_D are negative in case of a p-channel MOSFET.*

4.3.3 Output or Drain characteristics of MOSFET

I. Enhancement type n-channel MOSFET

The drain characteristics of MOSFET gives the variation of drain current (I_D) as a function of drain to source voltage (V_{DS}) and gate to source voltage (V_{GS}). Mathematically, the drain characteristics of a MOSFET are defined by,

$$I_D = f(V_{DS}, V_{GS}) \tag{112}$$

It has been seen in previous section the gate to source voltage is used to induce a conducting n-channel between source and drain regions. The n-channel forms the inversion layer of electrons below oxide layer between the source and drains regions of the MOSFET. Fig.25 shows the drain characteristics of an enhancement type n-channel MOSFET. The drain characteristics of MOSFET can be divided into three regions called ohmic, saturation and cutoff regions depending upon the value of gate to source and drain to source voltages.

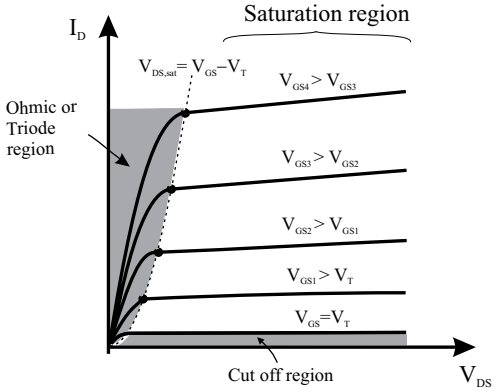


Fig. 25 Drain characteristics of n-channel enhancement type MOSFET

Ohmic or Triode or Linear region

When voltage (V_{GS}) applied between gate and source terminals is more than the threshold voltage, an inversion layer of electrons is induced in substrate region below gate electrode forming a conducting channel ash shown in Fig. 24. If drain to source voltage (V_{DS}) is increased from zero, the electrons in channel start drifting from source to drain. Since current flows in the direction opposite to that of electrons, therefore, a current called drain current (I_D) starts flowing through the channel from drain to source. The concentration of charge carriers in the channel increases with increase in the gate to source voltage. Therefore, the drain current increases with increase in V_{GS} as shown in the figure. When V_{DS} is increased within the range $0 < V_{DS} < (V_{GS} - V_T)$ there in increase of drift velocity of electrons in the channel and thus the drain current increase. This limiting value of $V_{DS} = (V_{GS} - V_T)$, defines a boundary between the ohmic and saturation region and it is denoted by as $V_{DS,sat}$. It should be observed from the Fig.25 that value of $V_{DS,sat}$ increases with increase in voltage V_{GS}. The slope of drain characteristic gives the conductance of the channel of MOSFET and it changes with change in voltage V_{GS} in the ohmic region. The conductance of the channel of MOSFET in ohmic region is proportional to the excess voltage $(V_{GS} - V_T)$. This excess voltage is known as overdrive voltage. Thus, in ohmic region of operation a MOSFET behaves like a voltage controlled resistor or voltage variable resistor(VVR). The resistance of MOSFET varies linearly with voltage V_{GS} in ohmic region so ohmic region is a also linear region.

In the switching applications such as digital circuits, a MOSFET behaves like a closed switch with a finite resistance in ohmic region of operation. Thus a MOSFET has a finite ON state resistance unlike a BJT which has negligible ON state resistance.

The drain current of enhancement type n-channel MOSFET in ohmic region is function of drain to source voltage as well as gate to source voltage and it is given by

$$\boxed{I_D = \mu_n C_{ox} \frac{\mathcal{W}}{L}[(V_{GS} - V_T)\, V_{DS} - \frac{1}{2} V_{DS}^2]} \qquad (113)$$

where, $\mathcal{W}$ is width of the channel, L is length of the channel, k is process transconductance parameter and V_T is threshold voltage of the MOSFET

It should be noted here that symbol '$\mathcal{W}$' used is width of channel in MOSFET.

Saturation Region or Active Region

When gate to source voltage is more than the threshold voltage and drain to source voltage is increased above the limiting value of $V_{DS,sat}$, the MOSFET enters into the saturation region of operation. The operation of MOSFET in saturation region can be explained by considering effect of voltage V_{DS} on channel depth as shown in Fig. 26. It can be observed from the Fig. 26 that the voltage V_{DS} appears across complete length, L, of the channel. If source terminal is taken at ground reference then drain to source voltage increases from 0 at source end to V_{DS} at drain end. If gate to source voltage is considered to be fixed at particular value, V_{GS} , then the voltage across complete length of the channel varies from V_{GS} at source end to $(V_{GS} - V_{DS})$ at drain end. The depth of channel is proportional to the voltage across the channel, therefore, the channel depth is maximum at the source end and minimum on drain end of the channel as shown in Fig. 26.

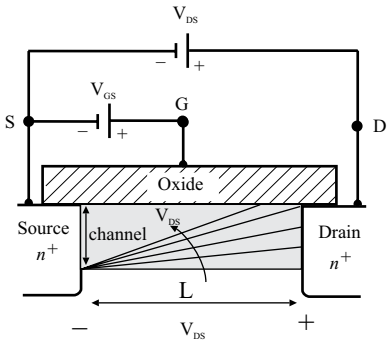


Fig. 26 Effect of V_{DS} in channel depth in n-channel enhancement type MOSFET

Thus channel acquires a *tapered or wedge shape* when voltage V_{DS} is increased from zero. The depth of channel on drain end further reduces with increase in the voltage V_{DS} . When the voltage across the channel V_{GD} or $(V_{GS} - V_{DS})$ becomes equal to V_T or alternatively V_{DS} becomes equal to a limiting value equal to $V_{GS} - V_T$ ($= V_{DS,sat}$), the channel is pinched off and its depth becomes negligible at drain end the drain current reaches at saturation level. It can be seen from drain characteristics in Fig. 25 that the drain current no more varies with voltage V_{DS} for $V_{DS} > (V_{GS} - V_T)$ because the channel is under pinched off condition for this voltage range. Thus, the drain current in saturation region is independent of drain to source voltage.

The drain current in saturation region is the function of gate to source voltage and it is given by

$$I_D = \mu_n C_{ox} \frac{W}{2L}(V_{GS} - V_T)^2 \qquad (114)$$

It is observed from above equation that the drain follows the square law relation with gate to source voltage and it is independent of drain to source voltage. In saturation region MOSFET can be used as an ideal current source whose value is controlled by V_{GS}. A MOSFET works like a transconductance amplifier in saturation region of operation.

Cut off region

The n-channel MOSFET works in cutoff region when gate to source voltage is less than the threshold

voltage. Therefore cutoff region is defined by,

$$\boxed{V_{GS} \leq V_T} \tag{115}$$

In cutoff region the drain current is negligible and MOSFET behaves like an open switch.

Note: Summary of conditions of operation of n-channel MOSFET in different regions of operation,

i. For ohmic region, $\boxed{V_{DS} < V_{GS} - V_T}$

ii. At boundary between ohmic and saturation regions, $\boxed{V_{DS} = V_{GS} - V_T}$

iii. For saturation region or pinched off region, $\boxed{V_{DS} > V_{GS} - V_T}$

iv. For cutoff region, $\boxed{V_{GS} \leq V_T}$

II. Enhancement type p-channel MOSFET

The output characteristics of enhancement type p-channel MOSFET are similar to that of enhancement type n-channel MOSFET as shown in Fig. 27. However, the voltages VGS, V_{DS} and current I_D are negative for a p-channel MOSFET.

The drain current enhancement type p-channel MOSFET in ohmic region is function of drain to source voltage as well as gate to source voltage and it is given by

$$\boxed{I_D = \mu_p C_{ox} \frac{W}{L}[(V_{SG} + V_T) V_{SD} - \frac{1}{2} V_{SD}^2]} \tag{116}$$

The drain current in saturation region is the function of gate to source voltage and it is given by

$$\boxed{I_D = \mu_p C_{ox} \frac{W}{2L}(V_{SG} + V_T)^2} \tag{117}$$

It should be noted here that mobility here is mobility of holes (μp)and sign of threshold voltage is reversed. The threshold voltage is negative for an enhancement type p-channel MOSFET.

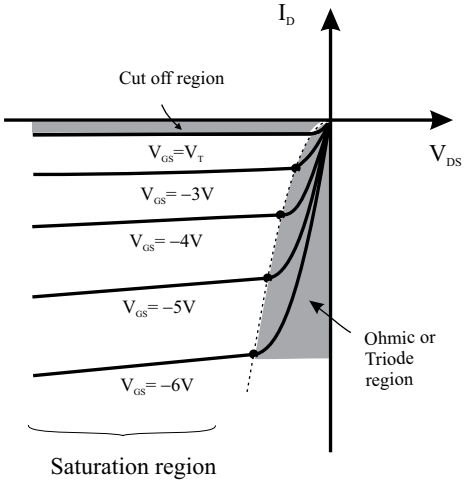


Fig. 27 Drain characteristics of p-channel enhancement type MOSFET

Note: Conditions for operation of p-channel MOSFET in different regions of operation,

i. For ohmic region PMOSFET, $V_{DS} > V_{GS} - V_T$ *or* $V_{SD} < V_{SG} - |V_T|$

ii. At boundary between ohmic and saturation regions,

$$V_{DS} = V_{GS} - V_T \quad or \quad V_{SD} = V_{SG} - |V_T|$$

iii. For saturation region or pinched off region,

$$V_{DS} < V_{GS} - V_T \quad or \quad V_{SD} > V_{SG} - |V_T|$$

iv. For cutoff region, $V_{GS} \geq V_T$ *or* $V_{SG} \leq |V_T|$

v. The voltages V_{DS}, V_{GS} *and* V_T *are negative for p-channel MOSFET.*

vi. The voltage difference $(V_{GS} - V_T)$ *is also known as Gate overdrive voltage.* (V_{OV})

III. Depletion type n-channel MOSFET

The depletion type MOSFETs are used rarely. The output characteristics of depletion type n-channel MOSFET are similar to that of enhancement type n-channel MOSFET as shown in Fig. 28. In depletion type of MOSFET the gate to source voltage can be positive or negative. When the gate voltage is positive the drain current increases with increase in the voltage so it works in enhancement mode and when gate to source voltage is negative and drain current decreases with gate voltage so it works in depletion mode. When a negative voltage is applied at gate terminal a depletion layer is formed in n-channel. The n-channel may be completely occupied by the depletion region at a critical gate voltage called pinch off voltage and drain current at pinch off becomes zero. This region of operation is called pinch off or cutoff region. So, the cutoff voltage for depletion type MOSFET is known as pinch off voltage.

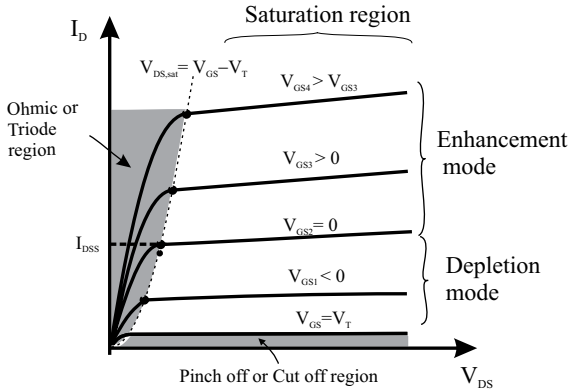


Fig. 28 Drain characteristics of n-channel depletion type MOSFET

The drain current in saturation region is the function of gate to source voltage and it is given by

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_T}\right)^2 \tag{118}$$

Where I_{DSS} is drain current when gate is short circuited with the source terminal and V_T is threshold

or pinch off voltage.

The current I_{DSS} for depletion type n-channel MOSFET is given by,

$$I_{DSS} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} V_T^2 \quad (118a)$$

Note : *i An n-channel depletion type MOSFET works in depletion mode when V_{GS} is negative and in enhancement mode when V_{GS} is positive.*

ii. A depletion type MOSFET can work in depletion as well as enhancement modes whereas the enhancement type MOSFET can work in enhancement mode only

Example 6

An enhancement-type NMOS transistor with $V_T = 0.7$ V has its source terminal grounded and a 1.5 V dc applied to the gate. In what region does the device operate for (i) $V_D = +0.5$ V (ii) $V_D = 3$V

Solution : (i) Triode ; (ii) Saturation;

Given, $V_T = 0.7$ V, $V_{GS} = 1.5$ V

$V_{GS} - V_T = 1.5 - 0.7 = 0.8$V

(i) $V_{DS} = 0.5$ V

NMOS works in ohmic region when $V_{DS} < (V_{GS} - VT)$.

So when $V_{DS} = 0.5$ V given NMOS operates in Triode or ohmic region.

(ii) $V_{DS} = 3$V

NMOS works in saturation region when $V_{DS} > (V_{GS} - V_T)$. So, for $V_{DS} = 3$V, the given NMOS works in saturation of operation.

4.3.4 Transfer characteristic of MOSFETs

Case-I: Transfer Characteristics of enhancement type n-channel MOSFET

Transfer characteristic of MOSFET gives the variation of output drain current with respect to the input gate to source voltage for a fixed drain to source voltage. The drain current varies differently with respect to gate to source voltage for ohmic and saturation regions therefore, a MOSFET has different transfer characteristics for ohmic and saturation regions.

Transfer characteristics for ohmic or linear region

The drain current for ohmic region of operation is given by,

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad (119)$$

For small value of V_{DS}, the drain current can be approximated as,

$$I_D = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS} \quad (120)$$

$$\Rightarrow \quad I_D = \mu_n C_{ox} \frac{W}{L} V_{DS} V_{GS} - \mu_n C_{ox} \frac{W}{L} V_T V_{DS} \tag{121}$$

$$\Rightarrow \quad I_D = mV_{GS} + c$$

The above equation represents of straight line in I_D Vs V_{GS} plane with a slope,

$$m = \mu_n C_{ox} \frac{W}{L} V_{DS} \tag{122}$$

It is observed here that I_D varies linearly with V_{GS} for fixed value of V_{DS} in ohmic region of operation. Practically curve varies nonlinearly due to source-drain resistance and mobility reduction at higher field across the oxide layer. The transfer characteristics for ohmic region is as shown in Fig. 29

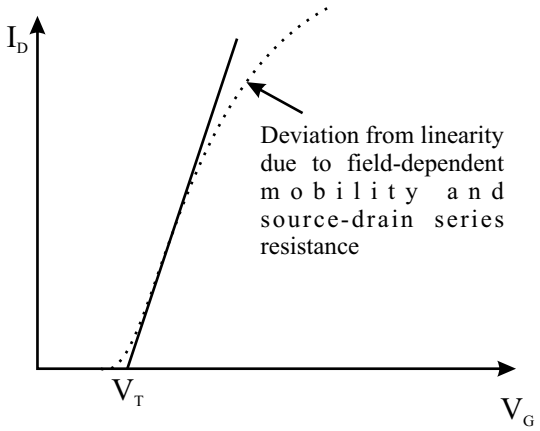


Fig. 29 Transfer characteristics of MOSFET in ohmic region

Transfer characteristics for saturation region

When the gate to source voltage is less then threshold voltage there exists depletion layer below oxide layer between source and drain which has no free charge carriers. An inversion layer of electron forms a conducting channel only when the gate to source voltage becomes more than the threshold voltage. The drain current of enhancement type MOSFET is negligible when gate voltage is less than threshold voltage.

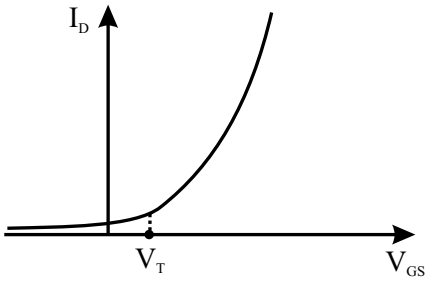


Fig. 30 Transfer characteristics of n-channel enhancement type MOSFET

The drain current starts increasing when the gate to source voltage V_{GS} is increased beyond the threshold voltage (V_T). The concentration of electrons in the channel increases with increase in gate to source voltage resulting into increase in the current. This mode of operation, where concentration of carriers increases in the channel with increase in gate to source voltage is called enhancement mode.

The drain current for saturation region of operation is given by,

$$I_D = \mu_n C_{ox} \frac{W}{2L}(V_{GS} - V_T)^2 \tag{123}$$

$$\Rightarrow \sqrt{I_D} = \sqrt{\mu_n C_{ox} \frac{W}{2L}}(V_{GS} - V_T)$$

$$\Rightarrow \sqrt{I_D} = \sqrt{\mu_n C_{ox} \frac{W}{2L}} V_{GS} - \sqrt{\mu_n C_{ox} \frac{W}{2L}} V_T$$

$$\Rightarrow \sqrt{I_D} = mV_{GS} + c \tag{124}$$

It is observed from above equation that I_D does not varies linear with V_{GS} in saturation region rather it follows the square law. However, $\sqrt{I_D}$ varies linearly with V_{GS} with a slope of

$$m = \sqrt{\mu_n C_{ox} \frac{W}{2L}} \tag{125}$$

The variation of $\sqrt{I_D}$ with respect to the voltage V_{GS} is shown in Fig. 31.

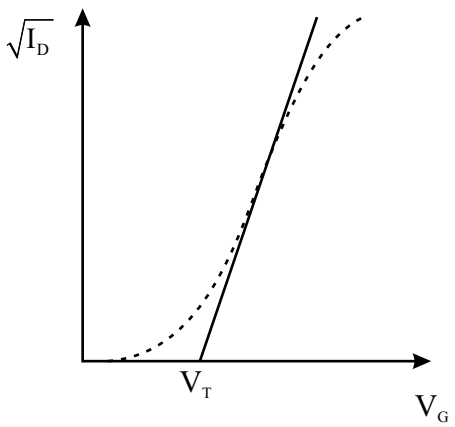


Fig. 31 Variation of $\sqrt{I_D}$ with respect to gate voltage of MOSFET in saturation region

Case-II Transfer characteristic of Depletion Type n-channel MOSFET

An depletion type n-channel MOSFET works in depletion mode when the gate to source voltage

is negative. The negative bias voltage induces a depletion layer in the n-type channel. The width of depletion layer increases and hence effective width of the channel reduces with increase in gate to source voltage. Therefore, the drain current reduces with increase in the gate to source voltage in depletion type n-channel MOSFET. At a critical voltage called pinch off voltage the conducting channel is completely covered by the depletion region and hence th drain current becomes also most zero. Such condition is known as pinch off condition. When the gate to source voltage is positive the electrons concentration in the channel increases and hence the drain current increases with increase in positive gate to source voltage. Such mode where drain current increases with increase in the positive gate to source voltage is called enhancement mode. The transfer characteristics of n-channel depletion type MOSFET are shown in Fig.32

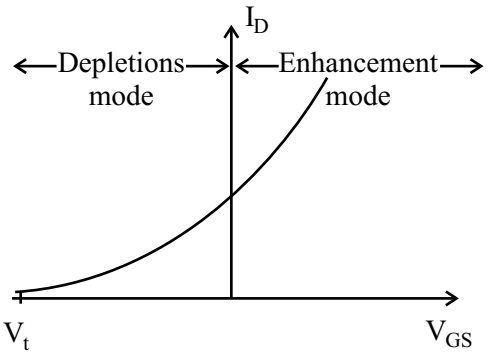


Fig. 32 Transfer characteristics of n-channel depletion type MOSFET

4.3.5 Control of Threshold Voltage of MOSFET

Since the threshold voltage determines the input voltage level required to turn on or turn off of a MOSFET, therefore, it should be adjustable. The threshold voltage of a MOSFET should be as kept low as possible because of the following reasons,

- Small power supply can be used.
- The device will have compatibility of operation with bipolar devices.
- It will require smaller switching time due to smaller voltage swing.
- Device will have higher packing density.

The threshold voltage of a n-channel MOSFET is given by

$$V_T = \frac{(Q_d + Q_x)}{C_{ox}} + 2\phi_F + \phi_{ms} \qquad (126)$$

where, $Q_d = qN_A W_{max} = \sqrt{4qN_A \in_s \phi_F}$ = bound charge density in depletion layer

Q_x = Positive charge trapped in oxide layer.

$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ = capacitance of oxide layer per unit area

From above equation it is observed that the threshold voltage can be reduced by using the following

methods.

i. By reducing work function difference (ϕ_{ms}) which can be reduced by using a poly-silicon gate doped with Boron instead of metal gate.

ii. The threshold voltage can be reduced by increasing the capacitance of oxide layer. The capacitance of oxide layer can be increased by reducing the dielectric thickness (t_{ox}) and by using oxide layer of ($Si_3 N_4$ + $Si O_2$) which has higher value of dielectric constant (ε_{ox}).

iii. The threshold voltage can also be reduced by ion implantation where ions of opposite polarity to that of substrate dopant are implanted near source and drain region in the channel. If dose of ion implantation is made heavy the behaviour of device can be changed from enhancement to depletion type which gives flexibility of fabricating both types of MOSFETs on same ICs. The threshold voltage can be reduced to zero with this technique. The ion implantation is basically used to neutralize the effect of unconverted impurities ions in depletion region below inversion layer of the MOSFET. the ion implantation also reduces C_{gd} and C_{gs}. The threshold voltage of n-channel enhancement type MOSFET with ion implantation with Boron ions can be given by,

$$V_{T2} = V_{T1} + \frac{qF_B}{C_{ox}} \qquad (127)$$

where, F_B is dose of Boron ions in the form of sheet of charge.

iv. By using silicon with <100> structure rather than <111> structure.

v. By reducing charge stored in the depletion layer which can be reduced by reducing the doping concentration of dopant in substrate.

vi. By connecting source at lower potential than the bulk.

Note

- *Threshold voltage of MOSFET is not kept at zero, practically, it is of order of 0.7 V.*
- *V_T for isolating regions should be kept high for proper isolation of devices.*
- *The threshold voltage reduces with reduction in channel length and it increases with reduction in channel width.*

Example 7

A silicon n MOSFET has a threshold voltage of 1 V and oxide thickness of $400A^0$.

[$\varepsilon_r(SiO2) = 3.9$, $\varepsilon_o = 8.854 \times 10^{-14}$ F/c.m. $q = 1.6 \times 10^{-19}$ C]

The region under the gate is ion implanted for threshold voltage tailoring. The dose and type of the implant (assumed to be a sheet charge at the interface) required to shift the threshold voltage to –1V are

(a) $1.08 \times 10^{12}/cm^2$, p-type

(b) $1.08 \times 10^{12}/cm^2$, n-type

(c) $5.4 \times 10^{11}/cm^2$, p-type

(d) $5.4 \times 10^{11}/cm^2$, n-type

GATE(EC/1996/2M)

Solution : Ans.(a)

Given,

Threshold voltage, $V_{T2} = -1V$, $V_{T1} = 1V$,

$\varepsilon_r(SiO2) = 3.9$,

$\varepsilon_o = 8.854 \times 10^{-14}$ F/cm,

Oxide thickness, $t_{ox} = 400\,\text{Å} = 400 \times 10^{-8}$ cm

Capacitance of oxide layer,

$$C_i = \frac{\varepsilon_{r,ox}\varepsilon_o}{t_{ox}}$$

Where C_i = Dielectric constant of oxide

F_B = Dose of ion-implanted

$$\therefore \quad C_i = \frac{3.9 \times 8.85 \times 10^{-12}}{40 \times 10^{-10}}$$

The threshold voltage with ion-implantation in n-MOSFET is given by,

$$V_{T2} = V_{T1} + \frac{qF_B}{C_i} \qquad \text{.....(i)}$$

Putting there values in equation (i), we have,

$$\Rightarrow \quad -1 = 1 + \frac{1.6 \times 10^{-19} \times F_B}{(8.854 \times 10^{-14} \times 3.9)/400 \times 10^{-8}}$$

$$\Rightarrow \quad F_B = 1.08 \times 10^{12}\ \text{cm}^{-2}$$

In n-channel MOSFET depletion layer consists of positive bound charges. These positive bound charges give positive threshold voltage. This threshold voltage can be made negative by ion-implantation with negative bound charge impurity of p-type material such as Boron.

Note :- *In n-channel MOSFET threshold voltage may be changed from positive to negative by changing stored charge in depletion layer from positive to negative.*

4.3.6 Derivation of I_D-V_{DS} Relationship of Enhancement type n-channel MOSFET

Consider an n-channel MOSFET connected with biasing voltages as shown in Fig.4.28. Let the voltage V_{GS} is more than the threshold voltage. The voltage V_{DS} appears across the channel with 0 V at the source end and V_{DS} at the drain end. Then effective voltage across the channel is $V_{GS} - V_{DS}$ at drain end and V_{GS} at source end. This difference in voltage across the conducting channel from source to drain end results in tapering of conducting channel with small depth on drain side as shown in Fig.33. Let the voltage drop from source to drain is V_x at distance x from the source end. Then the effective voltage across the channel is $V_{GS} - V_x$ at distance x from the source end of the channel.

Consider a differential portion dx of channel at distance x from the source end. If C_{ox} is capacitance per unit area of gate electrode then the capacitance of portion of dx is $C_{ox}\mathcal{W}dx$. The differential charge stored in inversion layer in differential portion dx of channel can be obtained by replacing voltage V_G by $V_{GS} - V_x$ in equation (103) as under,

$$dq = Q_{inv}\mathcal{W}dx = -C_{ox}\,\mathcal{W}.dx[V_{GS} - V_x - V_T] \qquad (128)$$

Where the negative sign indicates negative charge in inversion layer.

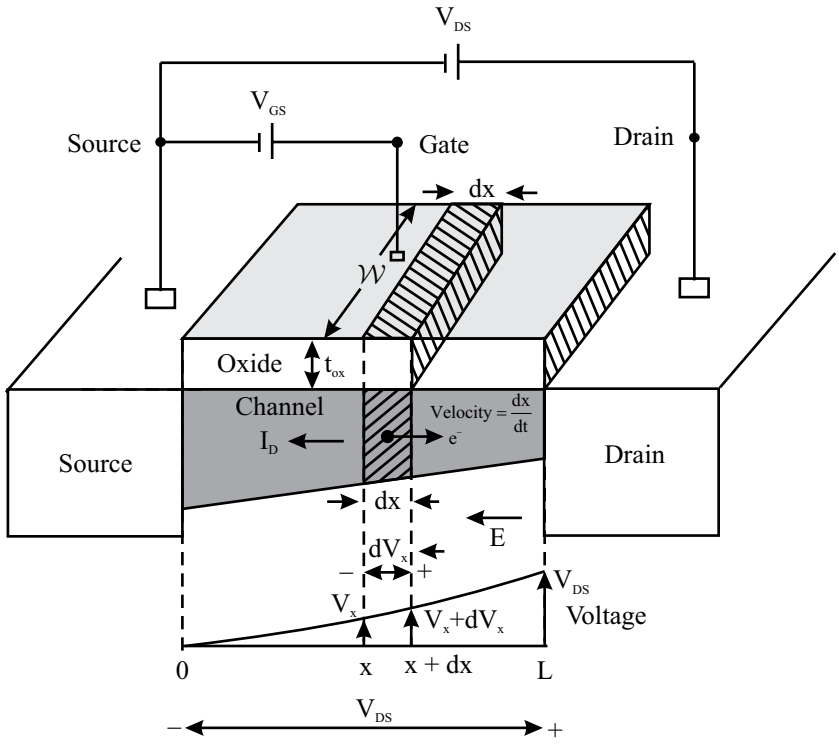


Fig. 33 n-channel MOSFET with zoomed channel region.

The electric field in channel is directed from drain to source in –x-direction due to voltage applied between drain and source. The voltage drop across the differential portion dx can be given by,

$$E_x = -\frac{dV_x}{dx} \tag{129}$$

The drift velocity of electrons from source to drain in the channel is related to the electric field as under,

$$\frac{dx}{dt} = -\mu_n E_x = \mu_n \frac{dV_x}{dx} \tag{130}$$

Negative sign in above equation indicates that the electrons move in the direction opposite to the direction of electric field.

Where μ_n is the mobility of electrons in the channel also known as surface mobility. It is a physical parameter whose value depends on the fabrication process technology. The surface mobility is normally less than the bulk mobility due to more scattering of electrons at surface region because of structural imperfections at the surface. The resulting drift current i in the channel can be given in the channel as follows :

$$I = \frac{dq}{dt} = \frac{dq}{dx} \times \frac{dx}{dt} \tag{131}$$

Putting charge dq and drift velocity dx/dt in above equation from equations (127) and (129) in above equation, we have,

$$I = -\mu_n C_{ox} \mathcal{W}\left[V_{GS} - V_x - V_T\right]\frac{dV_x}{dx}$$

The current i is measured at point 'x' in the channel but it is constant through out the channel of the MOSFET. So, the current 'I' must be equal to drain current of the MOSFET. Therefore, the drain current of MOSFET can be obtained as under,

$$I_D = -I = \mu_n C_{ox} \mathcal{W}\left[V_{GS} - V_x - V_T\right]\frac{dV_x}{dx}$$

$$\Rightarrow \quad I_D dx = \mu_n C_{ox} \mathcal{W}\left[V_{GS} - V_x - V_T\right]dV_x$$

Integrating both sides of over the range from x = 0 to x = L and corresponding values of V_x from 0 to V_{DS}, we have,

$$\int_0^L I_D dx = \int_0^{V_{DS}} \mu_n C_{ox} \mathcal{W}\left[V_{GS} - V_x - V_T\right]dV_x$$

$$I_D = (\mu_n C_{ox})\left(\frac{\mathcal{W}}{L}\right)\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right] \qquad (132)$$

The above expression of current I_D is applicable for linear region of drain characteristics. The drain to source voltage at the boundary of ohmic and saturation region, $V_{DS} = V_{GS} - V_T$, gives the drain current for saturation region as under,

$$\boxed{I_D = \frac{1}{2}(\mu_n C_{ox})\left(\frac{\mathcal{W}}{L}\right)(V_{GS} - V_T)^2} \qquad (133)$$

It is observed from above expression of current that the drain current for saturation region is independent of voltage V_{DS}.

Transconductance parameter

The factor $\mu_n C_{ox}$ is known as transconductance parameter of the MOSFET. It is determined by the process of fabrication of MOSFET. It is denoted by k for NMOS and has dimension of A/V^2.

$$\therefore \quad k = \mu_n C_{ox} \qquad (134)$$

The expressions of drain current for ohmic regions in terms of transconductance parameter can be written as follows :

Triode region:
$$I_D = k\frac{\mathcal{W}}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right] \qquad (135)$$

Saturation region:
$$\boxed{I_D = \frac{1}{2}k\frac{\mathcal{W}}{L}(V_{GS} - V_T)^2} \qquad (136)$$

The ratio of the channel width $\mathcal{W}$ to the channel length L in the expressions of drain current is known as the aspect ratio of the MOSFET. The voltage $V_{ov} = V_{GS} - V_T$ is called overdrive voltage of MOSFET.

Example 8

Consider an n-MOSFET for which $\varepsilon_{ox} = 4.5\times10^{-11}$ F/m, $t_{ox} = 8$ nm, $\mu_n = 450$ cm^2/V-s and $V_T = 0.7$ V. If W/L = 8 μm/0.8 μm then calculate the values of V_{GS} and $V_{DS\ min}$ needed to operate the transistor in the saturation region with a DC current $I_D = 100$ μA.

Solution :

Drain current in saturation region is given by,

$$I_D = \frac{\mu_n C_{ox} \mathcal{W}}{2L}(V_{GS} - V_T)^2 = \frac{\mu_n \varepsilon_{ox} \mathcal{W}}{2t_{ox} L}(V_{GS} - V_T)^2$$

Given, $I_D = 100\ \mu A = 100 \times 10^{-6}$ A

$\varepsilon_{ox} = 3.45 \times 10^{-11}$ F/m

$t_{ox} = 8$ nm $= 8 \times 10^{-9}$ m

$\frac{\mathcal{W}}{L} = 8\ \mu m/0.8\ \mu m = 10$

$V_T = 0.7V$

$\mu_n = 450$ cm^2 /V-s $= 450 \times 10^{-4}$ m^2/V-s

$\therefore \quad 100 \times 10^{-6} = \frac{450\times10^{-4}\times3.45\times10^{-11}\times10}{2\times8\times10^{-9}}(V_{GS} - 0.7)^2$

$\Rightarrow \quad V_{GS} = 1.021V$

Minimum drain to source voltage required to operate MOSFET is saturation region is given by,

$$V_{DS,\ min} = V_{GS} - V_T = 1.021 - 0.7 = 0.321V$$

Example 9

When the gate-to-source voltage (V_{GS}) of a MOSFET with threshold voltage of 400 mV, working in saturation is 900 mV, the drain current is observed to be 1 mA. Neglecting the channel width modulation effect and assuming that the MOSFET is operating at saturation, the drain current for an applied V_{GS} of 1400 mV is

(a) 0.5 mA (b) 2.0 mA

(c) 3.5 mA (d) 4.0 mA

GATE(EC/2003/2M)

Solution : Ans.(d)

Drain current of MOSFET is given by

$$I_D = K (V_{GS} - V_T)^2$$

Given, $I_D = 1$ mA at $V_{GS} = 900$ mV

& $V_T = 400$ mV

$\Rightarrow \quad 1 \times 10^{-3} = K(900 \times 10^{-3} - 400 \times 10^{-3})^2$

$\Rightarrow \quad K = \frac{1}{250}$

When, $V_{GS} = 1400$ mV

$\Rightarrow \quad I_D = \frac{1}{250}(1400 \times 10^{-3} - 400 \times 10^{-3})^2$

$\Rightarrow \quad I_D = 4$ mA

Example 10

Consider a long-channel MOSFET with a channel length 1 μm and width 10 μm. The device parameters are acceptor concentration $N_A = 5 \times 10^{16}$ cm^{-3}, electron mobility $\mu_n = 800$ cm^2/V-s, oxide capacitance/area $C_{ox} = 3.45 \times 10^{-7}$ F/cm^2, threshold voltage $V_T = 0.7$ V. The drain saturation current (I_{Dsat}) for a gate voltage of 5 V is_____mA (rounded off to two decimal places). [$\varepsilon_0 = 8.854 \times 10^{-14}$F/cm, $\varepsilon_{si} = 11.9$].

GATE(EC/2019/2M)

Solution : Ans.(25.40 to 25.60)

The drain current in saturation region of operation is given by,

$$I_{D,sat} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L}(V_{GS} - V_T)^2$$

Given, $V_{GS} = 5V, V_T = 0.7V$

$W = 10\ \mu m, L = 1\mu m$

$\mu_n = 800\ cm^2/V\text{-}s = 800 \times 10^{-4}\ m^2/V\text{-}s$

$C_{ox} = 3.45 \times 10^{-7}\ F/cm^2 = 3.45 \times 10^{-3}\ F/m^2$

$\therefore \quad \mu_n C_{ox} = 800 \times 10^{-4} \times 3.45 \times 10^{-3} = 2.76 \times 10^{-4}$

$\therefore \quad I_{D,sat} = \frac{2.76 \times 10^{-4}}{2} \times \frac{10 \times 10^{-6}}{1 \times 10^{-6}} \times (5 - 0.7)^2 = 25.51$ mA**3.7**

Transconductance of Enhancement type n-channel MOSFET

The transconductance of MOSFET is defined as change in drain current with respect to change in gate to source voltage. Mathematically, the transconductance region is given by,

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}}$$

Case-I : For ohmic region

The drain current in ohmic region of operation is given by,

$$I_D = \mu_n C_{ox} \frac{\mathcal{W}}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right] \quad (137)$$

Transconductance, $$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L} V_{DS} \quad (138)$$

Case-I : For saturation region

The drain current for saturation region is given by,

$$I_D = \frac{\mu_p C_{ox} \mathcal{W}}{2L} (V_{SG} - |V_T|)^2 \quad (139)$$

The transconductance, $$g_m = \frac{\partial}{\partial V_{SG}} \left[\mu_p C_{ox} \frac{W}{2L} [(V_{SG} - |V_T|)^2] \right]$$

$$\Rightarrow \quad \boxed{g_m = \mu_p C_{ox} \frac{\mathcal{W}}{L} (V_{SG} - |V_T|)} \quad (140)$$

It is observed from the above equation that g_m is linear function of gate voltage with zero value at $V_{GS} = V_T$. But practically the variation of transconductance is as shown in Fig. 34. The transconductance reaches a maximum value and then decreases due to effect of source-drain resistance and reduction in mobility at higher field across the oxide layer.

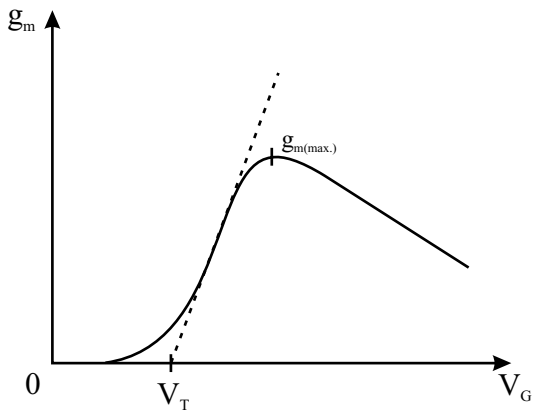


Fig. 34 Variation of g_m to gate voltage of MOSFET in saturation region

It is observed from above equation that the transconductance in saturation region is linear function of voltage V_{GS} and it is independent of voltage V_{DS}.

It is observed from equation (140) that the transconductance of MOSFET,

- Increases with increase in width of channel
- Increases with increase in electron mobility
- Increases with increase in capacitance per unit area of oxide
- Increases with increase in dielectric constant of oxide
- Decreases with increase in oxide thickness
- Decreases with increase in channel length.

Transconductance of Enhancement Type p-channel MOSFET

The drain current for saturation region of PMOS is given by,

$$I_D = \frac{\mu_p C_{ox} W}{2L}(V_{SG} - |V_T|)^2 \quad (141)$$

The transconductance, $$g_m = \frac{\partial}{\partial V_{SG}}\left[\mu_p C_{ox}\frac{W}{2L}[(V_{SG} - |V_T|)^2]\right]$$

$$\Rightarrow \quad \boxed{g_m = \mu_p C_{ox}\frac{W}{L}(V_{SG} - |V_T|)} \quad (142)$$

Transconductance of Depletion Type n-channel MOSFET

The drain current of n-channel depletion MOSFET is given by,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_t}\right)^2 \quad (143)$$

Where, I_{DSS} is drain current when gate terminal is shorted with source terminal. The current I_{DSS} is given by,

$$I_{DSS} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}V_t^2 \quad (144)$$

Transconductance, $$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\partial}{\partial V_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_t}\right)^2\right]$$

$$\Rightarrow \quad g_m = -\frac{2I_{DSS}}{V_t}\left(1 - \frac{V_{GS}}{V_t}\right) = g_{mo}\left(1 - \frac{V_{GS}}{V_T}\right) \quad (145)$$

Where, $$g_{mo} = -\frac{2I_{DSS}}{V_T} = \frac{2I_{DSS}}{|V_T|} \quad (146)$$

Example 10

An n-channel depletion MOSFET has following two points on its I_D-V_{GS} curve :

(i) $V_{GS} = 0$ at $I_D = 12$ mA and

(ii) $V_{GS} = -6$ Volts at $I_D = 0$

Which of the following Q-points will give the highest trans-conductance gain for small signals ?

(a) $V_{GS} = -6$Volts (b) $V_{GS} = -3$Volts

(c) $V_{GS} = 0$ Volts (d) $V_{GS} = 3$ Volts

GATE(EC/2006/1M)

Solution : Ans.(d)

The drain current of n-channel depletion MOSFET is given by,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_t}\right)^2 \quad .....(i)$$

Given, $I_D = 12\text{ mA at } V_{GS} = 0$

Putting above values in equation (i), we have,

$$\Rightarrow \quad 12 = I_{DSS}\left(1-\frac{0}{V_t}\right)^2$$

$$\Rightarrow \quad I_{DSS} = 12\text{ mA} \qquad \text{.....(ii)}$$

Also, $V_{GS} = -6\text{V when } I_D = 0$

Putting above values in equation (i), a gain, we have,

$$0 = 12\left(1-\frac{(-6)}{V_t}\right)^2$$

$$\Rightarrow \quad V_t = -6\text{V} \qquad \text{.....(iii)}$$

Transconductance of depletion type MOSFET is given by

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\partial}{\partial V_{GS}}\left[I_{DSS}\left(1-\frac{V_{GS}}{V_t}\right)^2\right]$$

$$\Rightarrow \quad g_m = -\frac{2I_{DSS}}{V_t}\left(1-\frac{V_{GS}}{V_t}\right)$$

$$\Rightarrow \quad g_m = -\frac{2\times 12}{(-6)}\left[1-\frac{V_{GS}}{(-6)}\right]$$

$$\Rightarrow \quad g_m = 4\left[1+\frac{V_{GS}}{6}\right]$$

i. when $V_{GS} = -6\text{V}$

$$g_m = 4\left(1-\frac{6}{6}\right) = 0$$

ii. when $V_{GS} = -3\text{V}$

$$g_m = 4\left(1-\frac{3}{6}\right) = 2\text{mS}$$

iii. when $V_{GS} = 0,\ g_m = 4\left(1+\frac{0}{6}\right) = 4\text{mS}$

iv. when $V_{GS} = 3\text{ V},\ g_m = 4\left(1+\frac{3}{6}\right) = 6\text{mS}$

Example 11

The slope of the I_D vs. V_{GS} curve of an n-channel MOSFET in linear regime is $10^{-3}\ \Omega^{-1}$ at $V_{DS} = 0.1$ V. For the same device, neglecting channel length modulation, the slope of the $\sqrt{I_D}$ vs. V_{GS} curve (in $\sqrt{A}$ / V) under saturation regime is approximately_____

GATE(EC-III/2014/2M)

Solution:Ans . (0.06 to 0.08)

The drain current in linear region of operation of n-channel MOSFET is given by

$$I_D = \frac{\mu_n C_{ox} W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$\Rightarrow \quad I_D = \frac{\mu_n C_{ox} W}{L}V_{GS}V_{DS} - \frac{\mu_n C_{ox} W}{L}\left[V_T V_{DS} + \frac{1}{2}V_{GS}\right]$$

Slope of I_D Vs V_{GS} curve represented by above equation is given by,

$$m = \frac{\mu_n C_{ox} W}{L}V_{DS}$$

Given, $m = 10^{-3}\ \Omega^{-1}$ at $V_{GS} = 0.1V$

$$\Rightarrow \quad 10^{-3} = \frac{\mu_n C_{ox} W}{L} \times 0.1$$

$$\Rightarrow \quad \frac{\mu_n C_{ox} W}{L} = 10^{-2}$$

Drain current in saturation region is given by,

$$I_D = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_T)^2$$

$$\Rightarrow \quad \sqrt{I_D} = \sqrt{\frac{\mu_n C_{ox} W}{2L}}V_{GS} - \sqrt{\frac{\mu_n C_{ox} W}{2L}}V_T$$

$\therefore$ Slope of $\sqrt{I_D}$ Vs V_{GS} curve represented by above equation,

$$m = \sqrt{\frac{\mu_n C_{ox} W}{2L}} = \sqrt{\frac{10^{-2}}{2}} = \frac{10^{-1}}{\sqrt{2}} = 0.0707$$

4.3.7 Channel Resistance in ohmic region or ON resistance of n-channel MOSFET

The channel resistance of MOSFET in ohmic region is also known as drain or output resistance. It can be obtained from expression of drain current of n-channel MOSFET (NMOS) for ohmic region as follows,

$$I_D = \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2] \quad (147)$$

Drain conductance, $$g_D = \frac{\partial I_D}{\partial V_{DS}} = \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_T) - V_{DS}] \quad (148)$$

When $V_{DS} << (V_{GS} - V_T)$, the drain current can be approximated by neglecting the term containing V_{DS} in above as under,

$$\boxed{g_D = \frac{\partial I_D}{\partial V_{DS}} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)} \quad (149)$$

Drain or channel resistance,

$$\boxed{r_D = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)}} \quad (150)$$

It is observed from above equation that the drain or channel resistance decreases linearly with increase in the gate to source voltage in ohmic region of operation. Therefore, MOSFET can be used as a voltage variable resister (VVR) in ohmic region of operation.

Note : The channel resistance in saturation region is infinite because the channel is in pinched off condition in saturation region of operation.

Example 12

Consider a long-channel NMOS transistor with source and body connected together. Assume that the electron mobility is independent of V_{GS} and V_{DS}. Given,

$g_m = 0.5$ μA/V for $V_{DS} = 50$ mV and $V_{GS} = 2$ V,

$g_d = 8$ μA/V for $V_{GS} = 2$ V and $V_{DS} = 0$ V

Where $\frac{\partial}{\partial}_{GS}$ and $g_d = \frac{\partial I_D}{\partial V_{DS}}$

The threshold voltage (in volts) of the transistor is .....

GATE(EC-II/2016/2M)

Solution : Ans. (1.18 to 1.22)

The NMOS operates in ohmic region when $V_{DS} = 0$.

The drain current in ohmic region of operation is given by,

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2\right]$$

Transconductance of transistor,

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L} V_{DS}$$

Given, $g_m = 0.5\ \mu A/V$ for $V_{DS} = 50\ mV$ and $V_{GS} = 2\ V$

$$\Rightarrow \quad 0.5\times10^{-6} = \mu_n C_{ox} \frac{\mathcal{W}}{L} \times 50\times10^{-3}$$

$$\Rightarrow \quad \mu_n C_{ox} \frac{\mathcal{W}}{L} = 0.01\times10^{-3}$$

Drain conductance of in ohmic region,

$$g_d = \frac{\partial I_D}{\partial V_{DS}} = \mu_n C_{ox} \frac{\mathcal{W}}{L}\left[(V_{GS} - V_T) - V_{DS}\right]$$

Given, $g_d = 8\ \mu A/V$ for $V_{GS} = 2\ V$ and $V_{DS} = 0\ V$

$$\Rightarrow \quad 8\times10^{-6} = 0.01\times10^{-3}\left[(2 - V_T) - 0\right]$$

$$\Rightarrow \quad V_T = 1.2\ V$$

Example 13

Consider an n-MOSFET for which $\varepsilon_{ox} = 4.5\times10^{-11}$ F/m, $t_{ox} = 8$ nm, $\mu_n = 450\ cm^2/V\text{-}s$ and $V_T = 0.7$ V. If W/L = 8 μm/0.8 μm then find the value of V_{GS} required to cause the device to operate as a 1000 Ω resistor for very small V_{DS}.

Solution:

An n-MOSFET can be operated as a resistor in ohmic region of operation. The resistance of MOSFET in ohmic region is given by,

$$r_D = \frac{1}{\mu_n C_{ox} \frac{\mathcal{W}}{L}(V_{GS} - V_T)} = \frac{1}{\mu_n \varepsilon_{ox} \frac{\mathcal{W}}{t_{ox} L}(V_{GS} - V_T)}$$

Given, $\mu_n = 410\ cm^2/V\text{-}s = 450 \times 10^{-4}\ m^2/V\text{-}s$, $\varepsilon_{ox} = 3.45 \times 10^{-11}$ F/m , $t_{ox} =$ 8 nm $= 8 \times 10^{-9}$ m

$$V_T = 0.7V$$

$$\frac{\mathcal{W}}{L} = \frac{8\mu m}{0.8\mu m} = 10$$

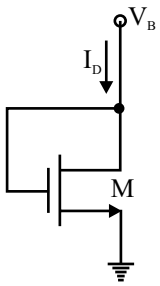
$$r_D = 1000\ \Omega$$

$$\Rightarrow \quad 1000 = \frac{1}{\frac{450\times10^{-4}\times3.45\times10^{-11}\times10}{8\times10^{-9}}(V_{GS} - 0.7)}$$

$$\Rightarrow \quad V_{GS} = 1.22\ V$$

Example 14

The small-signal resistance (i.e., dV_B/dI_D) in kΩ offered by the n-channel MOSFET M shown in the figure below, at a bias point of $V_B = 2$ V is (device data for M: device transconductance parameter $k_N = \mu_n C_{ox}'$ $(W/L) = 40\ \mu A/V^2$, threshold voltage $V_T = 1$V, and neglect body effect and channel length modulation effects)

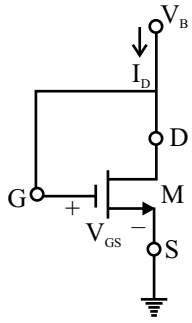


(a) 12.5 (b) 25

(c) 50 (d) 100

GATE(EC/2013/2M)

Solution : Ans.(b)



When gate terminal of MOSFET is shorted with the drain,

$$V_{DS} = V_{GS}$$

$$\therefore \quad V_{DS} > V_{GS} - V_T$$

The MOSFET operates in saturation region when $V_{DS} > V_{GS} - V_T$. The drain current of MOSFET in ohmic region is given by,

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2$$

Here, $V_{GS} = V_{DS} = V_B$

$$\Rightarrow \quad I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_B - V_T)^2$$

Differentiating w.r.t. V_B, we have,

$$\frac{dI_D}{dV_B} = \mu_n C_{ox} \frac{W}{L}(V_B - V_T)$$

Given, $\mu_n C_{ox} \cdot \frac{W}{L} = 40\ \mu A/V^2 ; V_B = 2V ;$

$$V_T = 1V$$

$$\Rightarrow \quad \frac{dI_D}{dV_B} = 40 \times 10^{-6}(2-1) = 40 \times 10^{-6} \text{ mho}$$

Small signal resistance of MOSFET,

$$\frac{dV_B}{dI_D} = \frac{1}{40\times10^{-6}} = \frac{1000}{40}k\Omega = 25k\Omega$$

4.3.8 Non-ideal Effects in MOSFETs

I. Channel Length Modulation Effect

It has been assumed till now that the voltage V_{DS} does not affect the drain current in saturation region once the conducting channel is pinched off for $V_{DS} > V_{GS} - V_T$. However, practically the effective channel length reduces with in V_{DS} as shown in Fig.35.

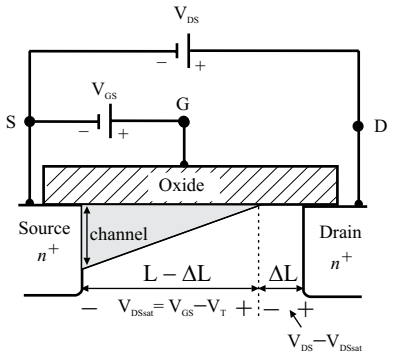


Fig. 35 Channel length modulation in n-channel MOSFET

When V_{DS} is increased above $V_{GS} - V_T$ the pinched off region of channel expands towards source region and effective length of channel reduces from L to L–ΔL. This phenomenons is known as channel length modulation. As drain current is inversely proportional to L so it increases with decrease in L. The drain current when effective channel length is L–ΔL can be given by,

$$I_D = \frac{1}{2}k\frac{W}{L-\Delta L}(V_{GS} - V_T)^2 \qquad (151)$$

$$\Rightarrow \quad I_D = \frac{1}{2}k\frac{W}{L}\frac{1}{1-\frac{\Delta L}{L}}(V_{GS} - V_T)^2$$

$$\Rightarrow \quad I_D = \frac{1}{2}k\frac{W}{L}\cdot\left(1-\frac{\Delta L}{L}\right)^{-1}(V_{GS}-V_T)^2 \tag{152}$$

If $\Delta L << L$ then $\left(1-\frac{\Delta L}{L}\right)^{-1} \approx \left(1+\frac{\Delta L}{L}\right)$ as probational expansion.

$$\Rightarrow \quad I_D = \frac{1}{2}k\frac{W}{L}\left(1+\frac{\Delta L}{L}\right)(V_{GS}-V_T)^2 \tag{153}$$

The fractional change in channel length $\Delta L/L$ is proportional to the voltage V_{DS} and it can be given as

$$\Delta L/L = \lambda V_{DS} \tag{154}$$

Where λ is called channel length modulation parameter or channel length modulation coefficient.

$$\Rightarrow \quad \boxed{I_D = \frac{1}{2}k\frac{W}{L}(1+\lambda V_{DS})(V_{GS}-V_T)^2} \tag{155}$$

It is observed from the above equation that the drain current increases with increase in V_{DS} in saturation region also due to channel length modulation effect. The drain characteristics with channel modulation effect can be drain as shown in Fig.36. When output characteristics are extended backward, these meet at point $-V_A$ on V_{DS} - axis.

From above equation, $I_D = 0$ when $1 + \lambda V_{DS} = 0$

$$\Rightarrow \quad V_{DS} = -\frac{1}{\lambda} \tag{156}$$

Let the value of V_{DS} at $I_D = 0$ is equal to $-V_A$ then,

$$-V_A = -\frac{1}{\lambda}$$

$$\Rightarrow \quad V_A = \frac{1}{\lambda} \tag{157}$$

The voltage V_A is usually referred as early voltage.

The drain or channel or output conductance for saturation region with channel length modulation effect can be given as,

$$g_o = \frac{\partial I_D}{\partial V_{DS}} \tag{158}$$

$$\Rightarrow \quad g_o = \frac{1}{2}k\frac{W}{L}(V_{GS}-V_T)^2\cdot\frac{\partial(1+\lambda V_{DS})}{\partial V_{DS}}$$

$$\Rightarrow \quad g_o = \frac{1}{2} k \frac{W}{L} (V_{GS} - V_T)^2 \cdot \lambda = I_D' \lambda \tag{159}$$

where, $$I_D' = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2 \tag{160}$$

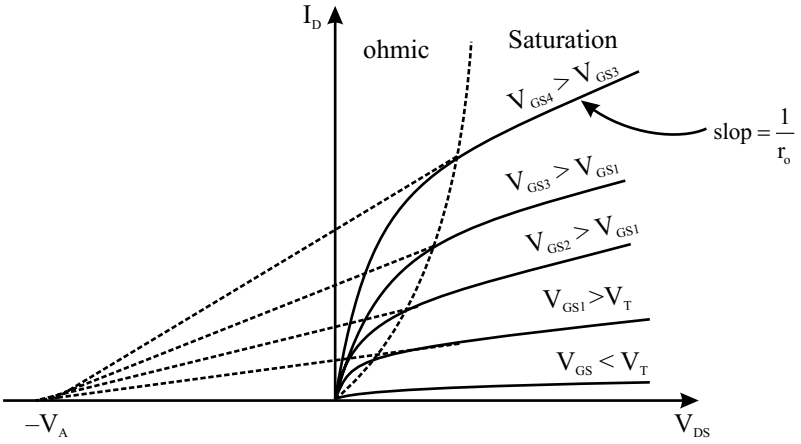


Fig. 36 Output characteristics of enhancement type n-channel MOSFET with channel length modulation

The current I_D' is drain current without channel length modulation effect taken into account.

Output or drain or channel resistance in saturation region,

$$r_o = \frac{1}{g_o} = \frac{1}{I_D' \lambda} = \frac{V_A}{I_D'} \tag{161}$$

Note : i. The drain current and output resistance for PMOS with channel length modulation effect is given by,

$$I_D = \frac{\mu_p C_{ox}}{2} \frac{W}{L} (1 + \lambda V_{DS})(V_{GS} - V_T)^2$$

Here, V_{DS}, V_{GS} and V_T are negative for PMOS

ii. The output resistance of PMOS with channel modulation effect is given by,

$$r_o = \frac{1}{g_o} = \frac{1}{I_D' \lambda} = \frac{|V_A|}{I_D'}$$

The current I_D' is drain current without channel length modulation effect taken into account.

II. Substrate Body Effect

In many applications, the body terminal of the MOSFET is shorted with source terminal which results in pn junction between substrate and channel having zero bias. In such cases substrate does not play any role in circuit operation and its existence can be neglected. However, in integrated circuits (ICs) the substrate is normally common to many MOS transistors. In such circuits, the substrate is normally connected to highest negative potential in order to maintain cutoff condition for

all substrate-to-channel pn junctions. The resulting reverse bias voltage V_{SB} between source and body results in widening of depletion region and reduction of the effective depth of conducting channel as shown in Fig.37.

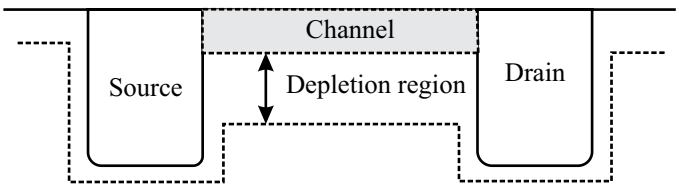


Fig. 37 Channel depth reduction due to substrate body effect.

The value of V_{GS} required to maintain the depth of the channel is more and the threshold voltage is also increased due to the body effect. The increase in threshold voltage results in decrease in drain current. Therefore, it is observed the negative potential given to the substrate of MOSFET controls the drain current also. Thus body acts like another gate for MOSFET and this phenomenon is known as body effect.

The change in threshold voltage due to substrate body effect for both n-channel and p-channel MOSFETs is given by,

$$\Delta V_T = \frac{\sqrt{2\varepsilon_s q N_A}}{C_i}\left[\left(2\phi_F + |V_B|\right)^{1/2} - \left(2\phi_F\right)^{1/2}\right]$$

Where, V_B is substrate bias voltage. It is negative for n-channel MOSFET and positive for p-channel MOSFET.

The variation in threshold voltage w.r.t. to variation in substrate bias voltage can be given by,

$$\therefore \quad \frac{\partial V_T}{\partial V_B} = \frac{1}{2}\frac{\sqrt{2\varepsilon_s q N_A}}{C_i}\left(2\phi_F + |V_B|\right)^{-\frac{1}{2}}$$

Here $2\phi_F << |V_B|$ and can be neglected.

III. Temperature Effect

The channel resistance in ohmic region is given by,

$$r_D = \frac{\partial V_{DS}}{\partial I_D} = \frac{L}{k\mathcal{W}\left(V_{GS} - V_T\right)} \tag{162}$$

The threshold V_T voltage has negative temperature coefficient of approximately –2 mV/°C. The transconductance parameter k also decreases with increase in temperature. Here the decrease in k w.r.t. temperature is more dominant over decrease in V_T with temperature, therefore, the channel resistance increases with increase in temperature. Hence, the channel resistance of MOSFET has positive temperature co-efficient unlike BJT which has negative temperature co-efficient. Therefore, the drain current of MOSFET decreases with increase in temperature which makes it suitable for parallel operation.

The drain current in FET deceases with increase in temperature due to decrease in mobility of carriers in the channel with increase in temperature of the device. The transconductance decreases with increase in temperature. The variations in drain resistance and transconductance with temperature are shown in Fig. 37b.

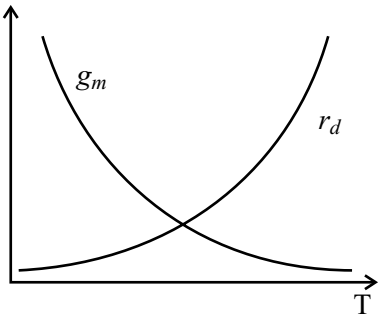


Fig. 37 (b) Variations of rd and gm of FET with temperature

Note : *i. Since MOSFET has positive temperature coefficient, therefore, its resistance increases with increase in temperature and drain current reduces, because of this characteristic FET never undergoes a thermal breakdown or secondary breakdown. This characteristic of FET makes it suitable for parallel operation.*

ii. BJT has negative temperature coefficient, therefore, it suffers from secondary or thermal breakdown. This characteristic of BJT makes it unsuitable for parallel operation.

IV. Sub-threshold current

When the gate voltage is less than the threshold voltage the drain current even exists due to existence of inversion layer for potential surface in the range, $\phi_F < \phi_s < 2\phi_F$. It has been seen in MOS capacitor the inversion layers starts forming when the surface potential, ϕ_s, becomes more than ϕ_F. This sub-threshold drain current is leakage current of MOSFET in OFF state. It results in power dissipation in MOSFET in OFF state.

The sub-threshold current is observed during weak invention when . It is kept as minimum as possible to reduce OFF state power lass in MOSFET.

V. Mobility variation

The mobility of electrons in inversion layer is smaller than bulk of semiconductor due to surface scattering. The carriers in the channel are very close to the semiconductor-oxide interface, they are scattered by surface roughness and by coulombic interaction with fixed charges in the gate oxide.

VI. Hot Electron Effect

The electrons traveling from source to drain in n-channel MOSFET acquires high kinetic energy in pinch-off region near drain on expense of energy stored in electrostatic potential in pinch off region. These electrons are called hot electrons. Hot electrons can jump from conduction band of semiconductor to the conduction band of oxide thus penetrate in the oxide layer. The hot electrons may result in increase in flat band and threshold voltages and give rise to a current in gate terminal resulting in reduction in input impedance of the MOSFET. This effect is known a hot electron effect. This effect is less prominent in p-channel MOSFET because the mobility of holes is less than that of electrons.

Example 15

A MOSFET in saturation has a drain current of 1 mA for $V_{DS} = 0.5$ V. If the channel length modulation coefficient is 0.05 V^{-1}, the output resistance (in kΩ) of the MOSFET is .....

GATE(EC-I/2015/2M)

Soluiton : Ans.(19 to 21)

The channel resistance in terms channel length modulation coefficient is given by,

$$r_o = \frac{1}{\lambda I_D}$$

where, I_D drain current without channel modulation effect and λ is channel length modulation coefficient.

Given, $\lambda = 0.05\ V^{-1}$ and $I_D = 1$ mA

$$\Rightarrow \quad r_o = \frac{1}{0.05 \times 1}\ k\Omega = 20\ k\Omega$$

Example 16

The current in an enhancement mode NMOS transistor biased in saturation mode was measured to be 1 mA at a drain-source voltage of 5V. When the drain-source voltage was increased to 6V while keeping gate-source voltage same, the drain current increased to 1.02 mA. Assume that drain to source saturation voltage is much smaller than the applied drain-source voltage. The channel length modulation parameter λ(in V^{-1}) is .....

GATE(EC-III/2015/2M)

Soluiton: Ans.(0.018 to 0.026)

The drain current in terms channel length modulation parameter is given by,

$$I_D = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS})$$

Case-I: When $V_{DS} = 5$V, $I_D = 1$ mA

$$\Rightarrow \quad 10^{-3} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} (V_{GS} - V_{th})^2 (1 + 5\lambda) \qquad .....(i)$$

Case-II: When $V_{DS} = 6$V, $I_D = 1.02$ mA

$$\Rightarrow \quad 1.02 \times 10^{-3} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} (V_{GS} - V_{th})^2 (1 + 6\lambda) \qquad .....(ii)$$

From the equations (i) and (ii), we have,

$$\frac{1.02}{1} = \frac{1 + 6\lambda}{1 + 5\lambda}$$

$$\lambda = 0.0222\ V^{-1}$$

Example 17

Consider an *n*-channel metal oxide semiconductor field effect transistor (MOSFET) with a gate-to source voltage of 1.8 V. Assume that $\frac{W}{L} = 4$, $\mu_N C_{ox} = 70 \times 10^{-6}\ AV^{-2}$, the threshold voltage is 0.3 V,

and the channel length modulation parameter is 0.09 V^{-1}. In the saturation region, the drain conductance (in micro seimens) is .....

GATE(EC-I/2016/2M)

Soluiton : Ans. (28 to 29)

The drain current in saturation region when the channel length modulation is taken into consideration is given by,

$$I_D = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

Drain conductance, $$g_D = \frac{\partial I_D}{\partial V_{DS}} = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_T)^2 \lambda$$

Given, $\frac{W}{L} = 4$, $V_{GS} = 1.8V$, $\mu_N C_{ox} = 70 \times 10^{-6}\ AV^{-2}$, $V_T = 0.3\ V$, $\lambda = 0.09\ V^{-1}$

$$\Rightarrow \quad g_D = \frac{70 \times 10^{-6} \times 4}{2}(1.8 - 0.3)^2 \times 0.09 = 28.35\ \mu S$$

4.3.9 MOSFET Scaling

The frequency response of a MOSFET increases as the channel length decreases. However, the while scaling of MOSFET the device dimension and voltages should be scaled such that both horizontal and vertical fields essentially remain constant. For example if channel length is changed from L to kL then the drain voltage should be changed from V_D to kV_D. Similarly the gate voltage is also changed from V_G to kV_G so that drain and gate voltages remain compatible to maintain vertical field constant, The oxide thickness should be changed from t_{ox} to kt_{ox}. The device scaling and its effects on various parameters of the device are shown in Table.1

Table 1: MOSFET Scaling and its effects on parameters

	Device and circuit parameters	Scaling factor(k < 1)
Scaled parameters	Device dimensions (L, $t_{ox,}$ W, x_i)	k
	Doping concentration (N_a, N_d)	1 / k
	Voltages	k
Effect on device parameters	Electric field	1
	Carrier velocity	1
	Depletion widths	k
	Capacitance (C = εA/t)	k
	Drift current	k
Effect on circuit parameters	Device density	$1 / k^2$
	Power density	1
	Power dissipation per device (P = VI)	k^2
	Circuit delay time (≈ CV/I)	k
	Power-delay product (Pτ)	k^3

4.3.10 Breakdown and Gate protection of MOSFET

Breakdown at Drain

The drain to substrate pn junction of MOSFET is reverse biased. If voltage at drain is increased beyond some critical value the pn junction between drain and substrate may breakdown due to avalanche multiplication. The avalanche multiplication results in sudden increase of drain current.

Another breakdown which occurs at low drain voltage before avalanche multiplication is punch through condition. The punch through occurs in devices with relatively smaller channel length where the depletion region of drain substrate pn junction extends towards the source region and completely covers the conducting channel between drain and source. The drain current increases suddenly. However, the breakdown due to punch through does not damage the device permanently.

Breakdown of Gate oxide

If gate to source voltage reaches critical value of approx 20V then there is dielectric breakdown of oxide layer which results in permanent damage to the device. The gate of MOSFET is protected by fabricating a Zener diode between gate and source. This diode protects the gate against excessively high voltage.

4.3.11 Comparison of Enhancement and Depletion type MOSFETs

i. An enhancement type MOSFET has no conducting channel when the gate voltage is zero whereas depletion type MOSFET has drain current even when gate voltage is zero. Therefore, depletion type of MOSFET is less preferred because it has less use in appliances.

ii. The logic level voltages of enhancement and depletion type of MOSFETs is opposite to each other.

iii. The depletion MOSFET is free from sub-threshold leakage current and gate oxide leakage current.

iv. As a enhancement MOSFET shrinking in size, there is no way to stop the sub threshold leakage current diffused across from source to drain because the drain and source terminals are closer physically. This is not the problem with depletion type MOSFET because a pinched channel stops the diffusion current completely.

4.3.12 Comparison between p-channel and n-channel MOSFET

i. p-channel has more ON state resistance as compared to n-channel.

ii. The physical size of p-channel MOSFET is more.

iii. Packing density of n-channel MOSFET is high.

v. n-channel MOSFET has better switching response.

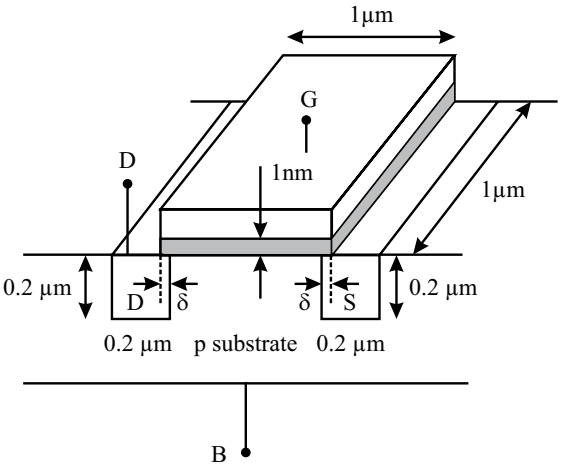
vi. Cost of n-channel is higher.

vii. n-channel MOSFET has the problem of premature turning ON due to contamination of positive ion in SiO_2 layer.

Example 18

Common Data for Questions A and B:

In the three dimensional view of a silicon n-channel MOS transistor shown below, $\delta = 20$ nm. The transistor is of width 1μm. The depletion width formed at every p-n junction is 10 nm. The relative permittivities of Si and SiO_2, respectively, are 11.7 and 3.9, and $\varepsilon_0 = 8.9 \times 10^{-12}$ F/m.



A. The source-body junction capacitance is approximately

(a) 2 fF (b) 7 fF

(c) 2 pF (d) 7 pF

B. The gate-source overlap capacitance is approximately

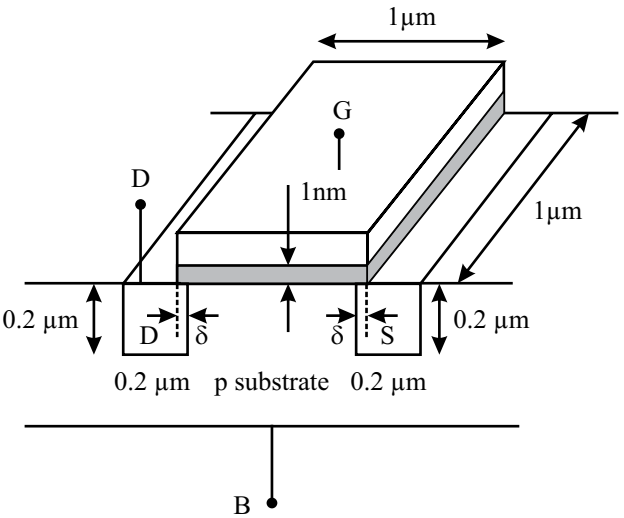
(a) 0.7 fF (b) 0.7 pF

(c) 0.35 fF (d) 0.24 pF

GATE(EC/2012/2M)

Solution:

A. Ans.(b)



Total area of cross-section of source w.r.t. substrate ,

$A_{ss} = (0.2 \times 10^{-6} + 0.2 \times 10^{-6} + 0.2 \times 10^{-6}) \times 1 \times 10^{-6}\ m^2 = 0.6 \times 10^{-12}\ m^2$

Width of depletion layer at junction between source & substrate, $W_s = 10 \times 10^{-9}$ m

Capacitance due to depletion layer is given as,

$$C_{ss} = \frac{\varepsilon_{r,si}\varepsilon_o A_{ss}}{W_{ss}} = \frac{11.7 \times 8.9 \times 10^{-12} \times 0.6 \times 10^{-12}}{10 \times 10^{-9}}$$

$$\Rightarrow \quad C_{ss} = 6.24 \times 10^{-15}\ F \approx 7\ fF$$

B. Ans.(a)

Area of overlap between gate & source,

$$A_{GS} = 1 \times 10^{-6} \times \delta = 1 \times 10^{-6} \times 20 \times 10^{-9}$$

$$\Rightarrow \quad A_{GS} = 20 \times 10^{-15}\ m^2$$

Thickness of oxide layer, $t_{ox} = 1 \times 10^{-9}$ m

Capacitance of overlap area between gate and source,

$$C_{as} = \frac{\varepsilon_{r,sio_2}\varepsilon_o A_{GS}}{t_{ox}} = \frac{3.9 \times 8.9 \times 10^{-12} \times 20 \times 10^{-15}}{1 \times 10^{-9}}$$

$$\Rightarrow \quad C_{as} = 0.69 \times 10^{-15}\ F \approx 0.7\ fF$$

4.4 Junction Field Effect Transistor (JFET) (No more in GATE syllabus)

The basic structure of a n-channel JFET is shown in Fig. 38. It consists of a n-type semiconductor bar where p_+ type is diffused on both sides of the bar. The JFET has three terminals called Gate (G), Source (S) and Drain(D). The region between to gate regions is called channel of JFET.

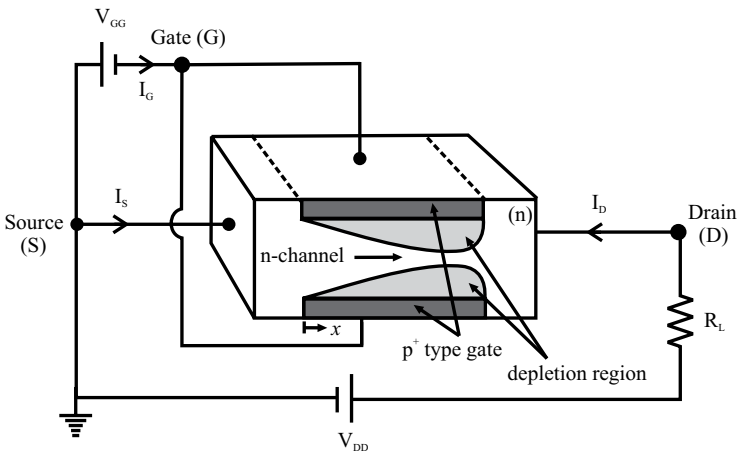


Fig. 38 Basic structure of n-channel JFET

Terminals of JFET :

1. **Source:** It is the terminal through which majority carriers enter into the channel of device. Source of FET is analogous to emitter of BJT.

2. **Drain:** Drain is the terminal through which majority carriers leave the channel of the device. It is analogous to collector of BJT.
3. **Gate:** It is the control terminal of the device. It is analogous to base of the BJT. In n-channel JFET a heavily doped p^+ region is defused on both sides of the *n*-channel to form the gate layer as shown in the figure.

Symbol of JFET :

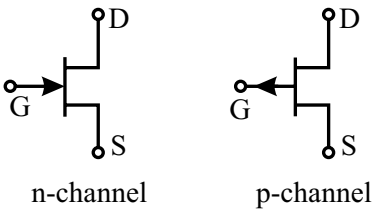


Fig. 39 Symbols of JFET

4.4.1 Operation of JFET

When pn junction formed on both sides of channel of JFET is reverse biased there is formation of depletion layer at the junction. As p^+ region of the gate is heavily doped as compared to the channel region so most of the depletion layer lies in the channel. The depletion layer has only immobile bound charges so it does not provide conduction path for the current. The width of depletion layer increases with increase in reverse biasing voltage applied at the gate terminal. The increase in depletion layer width results in decrease in effective width of the conducting channel which in turn results in decrease in channel conductance. Thus drain current of JFET decreases with increase in the reverse biasing voltage applied at the gate terminal of the device. Thus the modulation of channel conductance by gate voltage controls the channel current of the JFET. Therefore, JFET is a voltage controlled device. It can be used as a voltage controlled current source. The gate voltage induces a field in the depletion layer due to which name of devices is field effect transistor.

4.4.2 Static Drain Characteristics of JFET

The circuit of JFET with common source for static drain characteristics is shown in Fig.40.

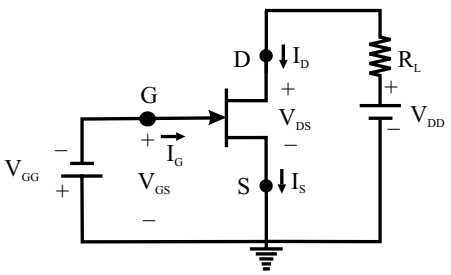


Fig. 40 Circuit of n-channel JFET for static drain characteristics

The drain characteristics of the n-channel JFET are drawn in the Fig. 41. The static drain characteristics of a JFET is defined by,

$$I_D = f(V_{DS}, V_{GS})$$

When the drain to source voltage,V_{DS}, is increased for a fixed value of gate to source voltage,V_{GS}, the drain current,I_D, initially increases linearly with voltage V_{DS} due to finite resistance offered by the channel. The width of depletion layer increases due to reverse bias of pn junction between gate and channel caused by voltage drop in the channel from drain to source. The potential drop is highest on drain end in n-channel JFET so the level of reverse bias is maximum on drain end of the channel and hence width of depletion layer is maximum and width of channel is smallest of drain end of the channel as shown in Fig. 38. When the drain to source voltage reaches at pinch off level the width of the channel reaches at minimum and drain current becomes constant and almost independent of V_{DS}. If voltage is further increased beyond some critical value an avalanche multiplication occurs at pn junction resulting in the breakdown and drain current increases suddenly. The drain to source voltage required for avalanche multiplication decreases with increase in gate to source reverse biasing voltage.

The drain to source voltage required for pinch off of the channel decreases with increase in gate to source reverse biasing voltage. When the gate to source reverse biasing voltage is increased the with of depletion layer decreases and channel width decreases. At a critical value of gate to source voltage called pinch off voltage, V_P, the channel width is reduced to zero and drain current becomes almost zero.

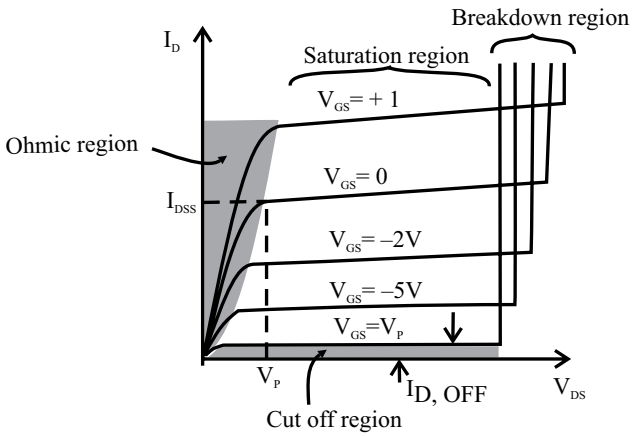


Fig. 41 Common source drain characteristics of n-channel JFET

Regions of operation

1. **Active/Saturation/Pentode region:** In saturation region the drain current, I_D, is almost constant and independent of drain to source voltage,V_{DS}. In this region the drain current varies with variation in gate to source voltage,V_{GS}. Therefore, JFET can be use as a transconductance amplifier in saturation region of operation. When gate to source reverse biasing voltage is increased the drain current reduces. At certain critical value of V_{GS} called **pinch off voltage,**V_P , the width of the

channel becomes negligible and drain current becomes almost zero. This condition corresponds to the pinch off condition and the device behaves like open switch. When drain current increases with increase in reverse biasing gate voltage the device operates depletion mode and when drain current increases with forward biasing gate voltage the device operates in enhancement mode. However, JFET is always used in depletion mode of operation.

2. **Ohmic/Triode region:** In ohmic region of operation, the device offers some finite resistance for particular value of gate to source voltage. As reverse biasing voltage at gate terminal is increase the width of depletion layer is increased and effective channel width is decreased and hence conductivity of channel is reduced. Thus, the resistance offered by the channel increases with increase in reverse biasing voltage V_{GS}. So, the device behaves like voltage variable resistor in ohmic region. In this region, JFET behaves like a closed switch having finite resistance. Because of the finite resistance offered by the device in ohmic region the ON state losses of FET are more than BJT. When the drain to source voltage is increased in ohmic region the drain current also increases proportionally. The drain current becomes almost constant when V_{DS} reaches a critical value called V_{DS} pinch off. The drain to source pinch off voltage reduces with increase in reverse biasing voltage V_{GS}.

3. **Cut-off region:** In this region the drain current is almost zero and the device behaves like an open switch. The gate to source voltage is equal to the pinch off voltage in cut off region. However, there is some leakage drain current, $I_{D,OFF}$, even under pinch off condition. The drain leakage current is of order of nanoamperes for a Si device.

4. **Breakdown region:** When drain to source voltage is increased beyond certain critical value, the drain current increases suddenly due to avalanche multiplication at reverse biased pn junction. This breakdown voltage reduces with increase in gate to source voltage.

Note : *i. FET can be used as a transconductance amplifier when it is operated in saturation.*

ii. FET can be used as a closed resistive switch in ohmic region and as an open switch in cut off region.

iii. FET can be used as a active load when drain is shorted with gate terminal.

iv. The maximum voltage that can be applied between any two teminals of FET is the lowest voltage that will cause avalanche multiplication.

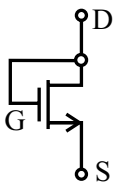


Fig. 42 FET used as load with gate shorted with the drain

4.4.3 Expression for pinch off voltage

The expression of pinch off voltage of a n-channel JFET can be obtained by consider a JFET operating in saturation mode as shown in Fig. 43. Let w is breadth of the channel, L is length of the channel, 2a is maximum width of the channel, 2b(x) is width of the channel at distance x from the edge of the channel and W(x) is width of depletion on one side of the channel corresponding to 2b(x).

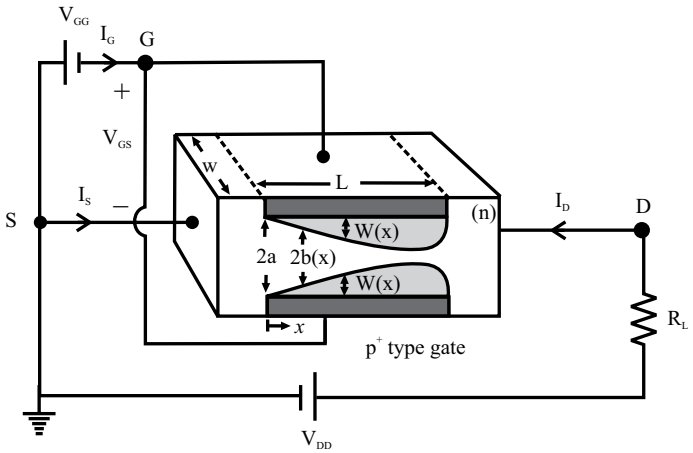


Fig. 43 Circuit for pinch off voltage of n-channel JFET

As p^+ layer of gate is heavily doped so most of the depletion layer lies in n-channel. The width of the depletion layer in the channel can be is given by,

$$W(x) = \sqrt{\frac{2\varepsilon}{q N_D}[V_o + V_{GS}(x)]} \tag{163}$$

where, N_D is donor concentration in the channel, ε is permittivity of semiconductor, is V_o barrier potential and $V_{GS}(x)$ is reverse biasing voltage at distance x from the left edge of the channel.

The total width of depletion layer at any distance 'x' from left edge of channel can be represented in terms of a & b as under,

$$2W(x) = 2a - 2b(x)$$

$$\Rightarrow \quad W(x) = a - b(x)$$

$$\Rightarrow \quad W = a - b(x) \tag{164}$$

From equations (163) and (164), we have,

$$a - b(x) = \sqrt{\frac{2\varepsilon}{q N_D}[V_o + V_{GS}(x)]} \tag{165}$$

At pinch off, $b(x) = 0$ and $V_o + V_{GS}(x) \approx V_P$

$$\therefore \quad a = \sqrt{\frac{2\varepsilon}{q N_D} V_P} \tag{166}$$

$$\Rightarrow \quad \boxed{V_P = \frac{q N_D}{2\varepsilon} . a^2} \qquad (167)$$

Relation between V_{GS} and V_P

The relation between V_{GS} and V_P can be obtained by putting $V_o + V_{GS} \approx V_{GS}$ in equation (165) as under,

$$a - b = \sqrt{\frac{2\varepsilon}{q} . \frac{1}{N_D} . V_{GS}} \qquad (168)$$

From equations (166) and (168), we have,

$$\Rightarrow \quad a - b = a\sqrt{\frac{V_{GS}}{V_P}} \qquad (169)$$

$$\Rightarrow \quad \boxed{V_{GS} = \left(1 - \frac{b}{a}\right)^2 . V_P} \qquad (170)$$

$$\Rightarrow \quad \boxed{b = a\left[1 - \left(\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}}\right]} \qquad (171)$$

4.4.4 Volt-ampare characteristic of JFET for ohmic region

The drain current for small voltage between drain and source can be given by

$$I_D = q(n\mu_n + p\mu_p)EA$$

Where, E is electric field in the channel and A is effective area of cross section of the channel.

For, n channel, $n \approx N_D$ and $n >> p$

$$\therefore \quad I_D \approx q N_D \mu_n EA \qquad (172)$$

Here, $$E = \frac{V_{DS}}{L} \qquad (173)$$

where, L is length of the channel.

The effective area of cross-section of the channel,

$$A = 2bw \qquad (174)$$

$$\Rightarrow \quad I_D = q N_D \mu_n \frac{V_{DS}}{L} \times 2bw \qquad (175)$$

Putting expression of b from equation (171) in above equation, we have,

$$\Rightarrow \quad \boxed{I_D = \frac{2aq N_D \mu_n w}{L}\left[1 - \left(\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}}\right] V_{DS}} \qquad (176)$$

It is observed from above equation that drain current, $I_D \propto V_{DS}$ in ohmic region, therefore, JFET

behaves like a resistance in ohmic region. This resistance is function of gate to source voltage V_{GS}. Therefore, device behaves like voltage controlled resistance. Because of this characteristic JFET can be used as a Voltage Variable Resistor (VVR) when it is operated in ohmic region.

Channel Resistance in ohmic region,

$$r_d = \frac{V_{DS}}{I_D} \tag{177}$$

$$\Rightarrow \quad r_d = \frac{r_{d,ON}}{1-\left(\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}}} \tag{178}$$

where,
$$r_{d,ON} = \frac{L}{2aq N_D \mu_n w} \tag{179}$$

The channel resistance $r_{d,ON}$ is ON state resistance of JFET. It is drain resistance at $V_{GS} = 0$. It is given by,

$$r_{d,ON} = \left.\frac{V_{DS}}{I_D}\right|_{V_{GS}=0} \tag{180}$$

The V-I characteristics of JFET for ohmic region are drawn in Fig.44. It is observed from equation (178) that the channel resistance of JFET increases with increase in gate to source voltage. Therefore, slope of the V-I character decreases with increase in gate to source voltage as shown in Fig. 44.

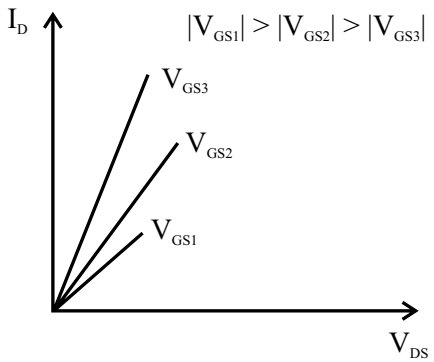


Fig. 44 Volt-ampare characteristic of JFET for ohmic region

Drain current in saturation region :

The electric field in channel, $E = \frac{V_{DS}}{L}$ (181)

The drain current in active region is almost independent of V_{DS} and it is given by:

$$I_D = 2aq N_D \mu_n WE\left[1-\left(\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}}\right] \tag{182}$$

The mobility of electrons is related to the electric field as under,

$$\mu_n \propto E^{-1} \quad ; E > 10^4 \text{ V/cm}$$

$$\propto E^{\frac{-1}{2}} \quad ; 10^3 < E < 10^4$$

$$= \text{constant} \quad ; E < 10^3$$

For saturation V_{DS} is large so the electric field is large. Therefore,

$$\mu_n \propto E^{-1}$$

or

$$\mu_n = kE^{-1} \text{ ; where k is constant of proportionality.} \quad (183)$$

$$\Rightarrow \quad I_D = 2kaq N_D W \left[1 - \left(\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}}\right] \quad (184)$$

It observed from this equation that the drain current becomes independent of voltage V_{DS} in saturation region.

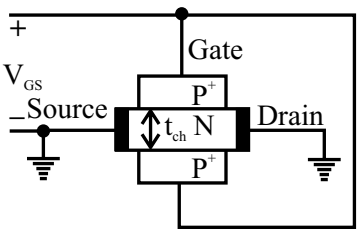
Note : *i. JFET behaves like ohmic device for small V_{DS} and like constant current source for large V_{DS} in saturation region.*

ii. FET has higher ON state resistance than BJT because it behaves like a resistor when it is operated as a closed switch in ohmic region. Therefore, continuous conduction losses are more in FET than a BJT. But switching losses in FET are less because it is a unipolar device and their is no reverse biased junction in the path of load current. So, the reverse recovery time of FET is negligible as compare to BJT. Due to which the losses during turning off are negligible. Since, the turn off time of FET is negligible due to negligible reverse recovery time, therefore, the switching frequency of FET is very high as compare to BJT.

Example 19

Common Data for Questions A and B:

The channel resistance of an N-channel JFET shown in the figure below is 600 Ω when the full channel thickness (t_{ch}) of 10 μm is available for conduction. The built-in voltage of the gate P^+N junction (V_{bi}) is – 1V. When the gate to source voltage (V_{GS}) is 0V, the channel is depleted by 1 μm on each side due to the built-in voltage and hence the thickness available for conduction is only 8 μm.



A. The channel resistance when $V_{GS} = 0$ V is

(a) 480 Ω (b) 600 Ω

(c) 750 Ω (d) 1000 Ω

B. The channel resistance when $V_{GS} = -3$ V is

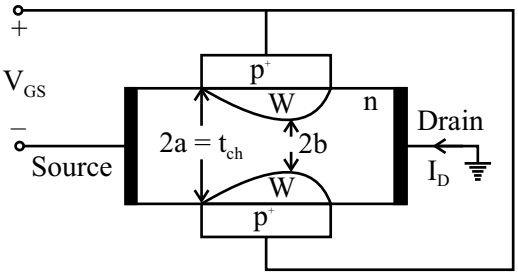
(a) 360 Ω (b) 917 Ω

(c) 1000 Ω (d) 3000 Ω

GATE(EC/2011/2M)

Solution:

A. Ans.(c)



Width of depletion layer,

$$W = a - b$$

where,

2a $\rightarrow$ Full channel thickness.

2b $\rightarrow$ Effective width of channel.

The drain current of JFET can be given by,

$$J_D = \sigma E \approx N_D q \mu_n \cdot \frac{V_{DS}}{L}$$

Let effective area of cross-section of channel,

$$A = 2bw$$

where, w $\rightarrow$ breadth of channel

$$\therefore \quad I_D = 2bWJ_D = 2bWN_D q\mu_n \frac{V_{DS}}{L}$$

Channel resistance for small values of V_{DS} in ohmic region,

$$\Rightarrow \quad r_d = \frac{V'_{DS}}{I_D} = \frac{L}{2bWN_D q\mu_n}$$

$$\Rightarrow \quad r_d \propto \frac{1}{2b}$$

$$\Rightarrow \quad r_{d2} = \frac{2b_1}{2b_2} \cdot r_{d1}$$

Given, $r_{d1} = 600\Omega$, $2b_1 = 10\mu m$, $2b_2 = 8\mu m$

$$\therefore \quad r_{d2} = \frac{10}{8} \times 600 = 750\Omega$$

B. Ans.(c)

Width of depletion layer in n-channel JFET is given by,

$$W = \sqrt{\frac{2\varepsilon}{q}\cdot\frac{1}{N_D}\cdot(V_o + V_{GS})}$$

Where, V_o is built in potential at pn-junction

$$\therefore \quad W \propto \sqrt{V_o + V_{GS}}$$

Given, W =1μm when $V_{GS} = 0$, $V_o = -1V$

When, $V_{GS} = -3V$

$$W_2 = \left[\frac{-1-3}{-1-0}\right]^{1/2} \times 1\ \mu m = 2\mu m$$

$\therefore$ Effective width of channel,

$$2b = 2a - 2W_2 = 10 - 4 = 6\ \mu m$$

Drain resistance, $r_{d3} = \frac{10}{6} \times 600 = 1000\ \Omega$

4.4.5 Transfer characteristics of JFET

JFET behaves like a constant current device in saturation region . In this region, the drain current is at saturation level and is independent of drain to source voltage but it varies as a function of gate to source voltage. The variation of drain current as a function of gate to source voltage in saturation region is called transfer characteristic. In saturation region, the drain current as a function of gate to source voltage is given by,

$$\boxed{I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2} \qquad (185)$$

where, I_{DSS} is drain current when $V_{GS} = 0$ i.e. gate is shorted to source. The transfer characteristics of JFET are as shown in Fig.45.

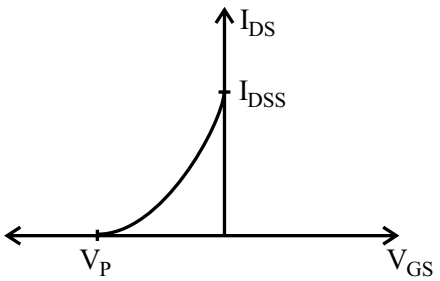


Fig. 45 Transfer characteristic of JFET

When $V_{GS} = V_P$, the drain current becomes '0' and device behaves like open switch. When drain to source voltage is increased with fixed V_{GS} applied, the drain current also increases and channel width reduces. The channel width never reduces to zero with increase in drain to source voltage because the

current density will become infinite. So, when V_{DS} is increased the channel width reaches a minimum level at a threshold value of V_{DS} and current becomes constant and the device enters into saturation region. This current in saturation region can be reduced to zero only by applying negative V_{GS} i.e. gate to source voltage equal to pinch off voltage. When V_{GS} is greater than V_P, a small leakage current flows through the device from drain to source. These current is called $I_{D,OFF}$. The current $I_{D,OFF}$ is order of nano-amperes.

Note : *Since the output drain current of FET is function of gate to source input voltage, therefore, FET is an example of voltage controlled current source.*

Gate reverse current (I_{GSS}):

This is the current which flows from gate to source when $V_{GS} > V_P$ with drain short circuited with source. The I_{GSS} is of order of nano-amperes for silicon.

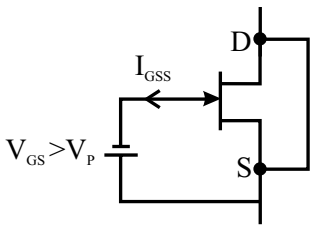


Fig. 46 Gate reverse current of JFET

Note : *FETs/MOSFETs are fabricated with silicon because:*

i) Wafer preparation is easy.
ii) Silicon is available in abundance.
iii) IC fabrication is easy with silicon.
iv) Many devices can be fabricated with single crystal layer.
v) Silicon can be used as a semiconductor when it is single crystal and it can be used as a insulator with SiO_2.
vi) It is stable at higher temperature.

4.4.6 Transconductance of JFET

The transconductance of JFET is defined as rate of change of drain current with respect to gate to source voltage for fixed value of drain to source voltage.

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{186}$$

Drain current of JFET for saturation region in terms of pinch off voltage is given by,

$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2 \tag{187}$$

$$\Rightarrow \quad g_m = \frac{\partial}{\partial V_{GS}}\left(I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2\right) = 2I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]\times\left(\frac{-1}{V_P}\right)$$

$$\Rightarrow \quad g_m = \frac{-2I_{DSS}}{V_P}\left[1-\frac{V_{GS}}{V_P}\right] \tag{188}$$

$$\Rightarrow \quad \boxed{g_m = g_{mo}\left[1-\frac{V_{GS}}{V_P}\right]} \tag{189}$$

where, $g_{mo} = -\frac{2I_{DSS}}{V_P}$ = Maximum Transconductance (190)

From equation (187), we have,

$$\left[1-\frac{V_{GS}}{V_P}\right] = \sqrt{\frac{I_{DS}}{I_{DSS}}} \tag{191}$$

Putting above relation in equation (188), we have,

$$\boxed{g_m = \frac{-2\sqrt{I_{DS}\,I_{DSS}}}{V_P} = 2\frac{\sqrt{I_{DS}\,I_{DSS}}}{|V_P|}} \tag{192}$$

Example 20

An n-channel JEFT has I_{DSS} = 2mA and V_P = –4 V. Its transconductance g_m (in millimho) for an applied gate to-source voltage V_{GS} of –2 V is

(a) 0.25 (b) 0.5

(c) 0.75 (d) 1.0

GATE(EC/1999/2M)

Solution : Ans.(b)

Transconductance of n-channel JFET is given by,

$$g_m = g_{m_o}\left[1-\frac{V_{GS}}{V_P}\right]$$

$$\Rightarrow \quad g_m = -\frac{2I_{DSS}}{V_P}\left[1-\frac{V_{GS}}{V_P}\right]$$

Given, I_{DSS} = 2 mA, V_P = –4 V

and V_{GS} = – 2V

$$\Rightarrow \quad g_m = -\frac{2\times 2}{-4}\left[1-\frac{(-2)}{(-4)}\right] \text{ millimho}$$

$$\Rightarrow \quad g_m = 0.5 \text{ millimho}$$

4.4.7 Small Signal Model of FET

The small signal model of a FET is represented in manner similar to a BJT. The drain current for small signal is formally represent as function of drain to source voltage and gate to source voltage as under,

$$i_D = f(v_{GS}, v_{DS}) \tag{193}$$

If both gate and drain voltages are variable then the drain current can be obtained by consider only first two terms of Taylor's series expansion, the drain current of FET can be given by

$$\Delta i_D = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{V_{DS}} \cdot \Delta v_{GS} + \left.\frac{\partial i_d}{\partial v_{DS}}\right|_{V_{GS}} \cdot \Delta v_{DS} \tag{194}$$

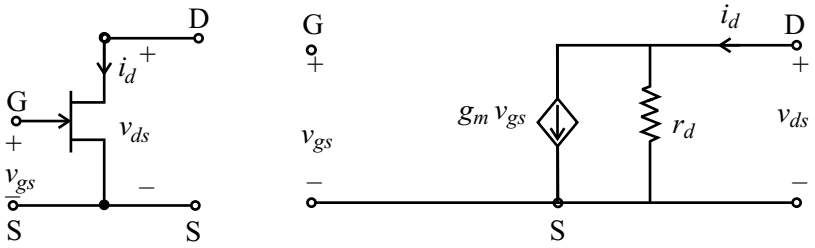
For small signals, $\Delta i_D = i_d$, $\Delta v_{DS} = v_{ds}$, $\Delta v_{GS} = v_{gs}$

$$\Rightarrow \quad \boxed{i_d = g_m v_{gs} + \frac{1}{r_o} . v_{ds}} \tag{195}$$

where, $g_m = \left.\frac{\delta i_d}{\delta v_{GS}}\right|_{V_{DS} = \text{constant}}$ and $r_d = \left.\frac{\delta v_{DS}}{\delta i_D}\right|_{V_{GS} = \text{constant}}$ (196)

The parameter g_m is called mutual conductance or transconductance of FET. It is also designated as common source forwarded transconductance. The second parameter r_d is drain resistance of the FET.

The small signal model of FET can be drawn by using equation (195) as as shown in Fig. 47.



(a) JFET (b) Small signal model

Fig. 47 Small signal model of FET

Small Signal Voltage Gain or Amplification Factor of FET

$$\mu = \frac{\partial v_{DS}}{\partial v_{GS}} = g_m r_d \tag{197}$$

Temperature Dependence of r_d and g_m

The drain current in FET deceases with increase in temperature due to decrease in mobility of carriers in the channel with increase in temperature of the device. The the drain resistance of FET increases with increase in temperature and transconductance decreases with increase in temperature. Thus, drain resistance of FET has positive temperature coefficient. The variations in drain resistance and transconductance with temperature are shown in Fig. 48.

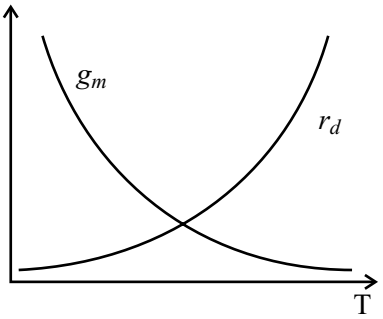


Fig. 48 Variations of rd and gm of FET with temperature

Note : *i. Since MOSFET has positive temperature coefficient, therefore, its resistance increases with increase in temperature and drain current reduces, because of this characteristic FET never undergoes a thermal breakdown or secondary breakdown. This characteristic of FET makes it suitable for parallel operation.*

ii. BJT has negative temperature coefficient, therefore, it suffers from secondary or thermal breakdown. This characteristic of BJT makes it unsuitable for parallel operation.

4.4.8 Comparison between JFET and MOSFET parameters

i. Transconductance gain (g_m) of MOSFET is more than JFET.

ii. Drain resistance (r_d)of JFET is of order of MΩ and that of MOSFET is of order of kΩ. JFETs have characteristic curves more flat than those of MOSFETs indicating a higher drain resistance due to low resistance offered by channel compared in JFET.

iii. Drain to source capacitance (C_{ds}) is of same order for both JFET and MOSFET

iv. Gate to source capacitance (C_{gs})an gate to drain capacitances (C_{gd}) are of same order.

v. Gate to source or input resistance (r_{gs}) of MOSFET is higher than that of JFET. This is due to negligibly small leakage current in MOSFET as compared to JFET.

vi. Gate to drain resistance (r_{gd}) of MOSFET is higher than that of JFET.

vii. JFETscanonlybeoperatedinthedepletionmodewhereasMOSFETscanbeoperatedineitherdepletion or in enhancement mode.

viii. When JFET is operated with a reverse bias on the junction, the gate current I_G is larger than it would be in a comparable MOSFET. The current caused by minority carrier extraction across a reverse-biased junction is greater, per unit area, than the leakage current that is supported by the oxide layer in a MOSFET. Thus MOSFET devices are more useful in electro-meter applications than are the JFETs.

ix. MOSFETs are somewhat easier to manufacture, they are more widely used than are the JFETs.

x. MOSFET has higher speed of operation compared to JFET's.

xi. Because the oxide layer is so thin, the MOSFET is susceptible to permanent damage by electrostatic charges. Even a small electrostatic build up can destroy a MOSFET permanently. But this can be avoided mostly by careful and intelligent design of the device.

❐❐❐

GATE QUESTIONS

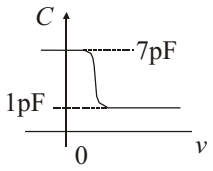
Q.1 A MOS capacitor made using p type substrate is in the accumulation mode. The dominant charge in the channel is due to the presence of

(a) holes (b) electrons

(c) positively charged ions (d) negatively charged ions

GATE(EC/2005/2M)

Q.2 The figure shows the high-frequency capacitance-voltage (C-V) characteristics of a Metal/SiO_2 / silicon (MOS) capacitor having an area of 1×10^{-4} cm^2. Assume that the permitivities $(\varepsilon_0\varepsilon_r)$ of silicon and SiO_2 are 1×10^{-12} F/cm and 3.5×10^{-13} F/cm respectively.



Consider the following statements about the C - V characteristics plot :

S1: The MOS capacitor has an n-type substrate.

S2: If positive charges are introduced in the oxide, the C-V plot will shift to the left.

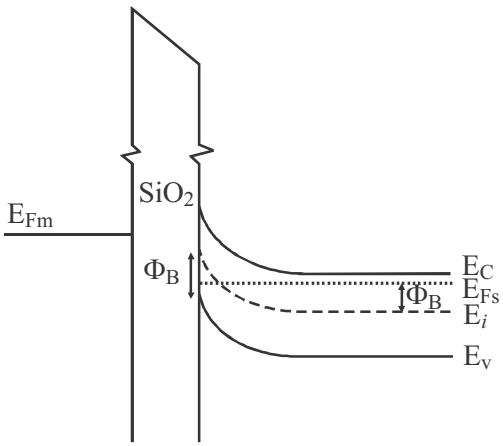
Then which of the following is true ?

(a) Both S1 and S2 are true (b) S1 is true and S2 is false

(c) S1 is false and S2 is true (d) Both S1 and S2 are false.

GATE(EC/2007/2M)

Q.3 The figure shows the band diagram of a Metal Oxide Semiconductor (MOS). The surface region of this MOS is in



(a) inversion (b) accumulation

(c) depletion (d) flat band

GATE(EC-III/2016/1M)

Q.4 Figures I and II show two MOS capacitors of unit area. The capacitor in Figure I has insulator materials X (of thickness t_1 = 1 nm and dielectric constant $\varepsilon_1 = 4$) and Y (of thickness t_2= 3 nm and dielectric constant $\varepsilon_2 = 20$). The capacitor in Figure II has only insulator material X of thickness t_{Eq}. If the capacitors are of equal capacitance, then the value of t_{Eq} (in nm) is .....

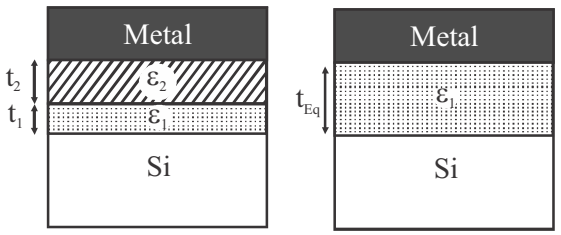
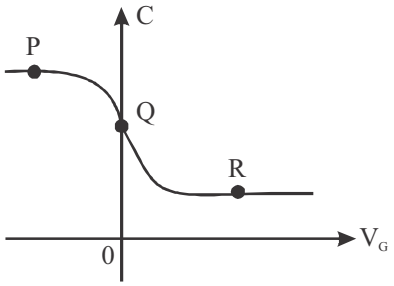


Figure I Figure II

GATE(EC-III/2016/2M)

Q.5 The figure shows the high-frequency C-V curve of a MOS capacitor (at T = 300 K) with Φ_{ms} = 0 V and no oxide charges. The flat-band, inversion, and accumulation conditions are represented, respectively, by the points



(a) P, Q, R (b) Q, R, P

(c) R, P, Q (d) Q, P, R

GATE(EC/2019/1M)

Q.6 Which of the following effects can be caused by a rise in the temperature ?

(a) Increase in MOSFET current (I_{DS}) (b) Increase in BJT current (I_c)

(c) Decrease in MOSFET current (I_{DS}) (d) Decrease in BJT current (I_c)

GATE(EC/1990/2M)

Q.7 The threshold voltage of an n channel MOSFET can be increased by

(a) Increasing the channel dopant concentration

(b) Reducing the channel dopant concentration

(c) Reducing the gat-oxide thickenss

(d) Reducing the channel length

GATE(EC/1994/1M)

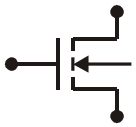
Q.8 The MOSFET switch in its on-state may be considered equivalent to

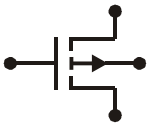
(a) Resistor (b) Inductor

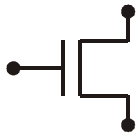
(c) Capacitor (d) Battery

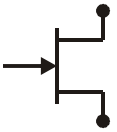
GATE(EE/1998|1-M)

Q.9 An enhancement type n-channel MOSFET is represented by the symbol

(a) 

(b) 

(c) 

(d) 

GATE(EE/1999|1 M)

Q.10 The effective channel length of a MOSFET in saturation decreases with increase in

(a) gate voltage (b) drain voltage

(c) source voltage (d) body voltage

GATE(EC/2001/1M)

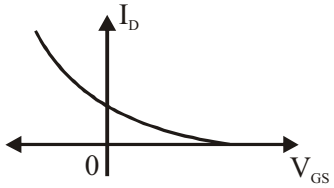
Q.11 MOSFET can be used as a

(a) current controlled capacitor (b) voltage controlled capacitor

(c) current controlled inductor (d) voltage controlled inductor

GATE(EC/2001/1M)

Q.12 The variation of drain current with gate-to-source voltage (I_D-V_{GS} characteristic) of a MOSFET is shown in Figure The MOSFET is



(a) an n-channel depletion mode device (b) a p-channel depletion mode device

(c) an n-channel enhancement mode device (d) a p-channel enhancement mode device

GATE(EE/2003|1 M)

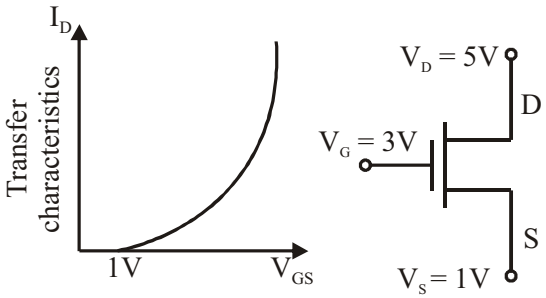
Q.13 For an n-channel enhancement type MOSFET, if the source is connected at a higher potential than that of the bulk (i.e.$V_{SB} > 0$), the threshold voltage V_T of the MOSFET will

(a) remain unchanged (b) decrease

(c) change polarity (d) increase

GATE(EC/2003/1M)

Q.14 For an n-channel MOSFET and its transfer curve shown in figure the threshold voltage is



(a) 1 V and the device is in active

(b) –1 V and the device is in saturation region

(c) 1 V and the device is in saturation region

(d) –1 V and the device is in active region

GATE(EC/2005/2M)

Q.15 Group I lists four different semiconductor devices. Match each device in Group I with its characteristic property in Group II

Group I	***Group II***
P. BJT inversion	1. Population
Q MOS capacitor	2. Pinch-off voltage
R LASER diode	3. Early-effect
S. JFET	4. Flat-band voltage

(a) P-3, Q-1, R-4, S-2

(b) P-1, Q-4, R-3, S-2

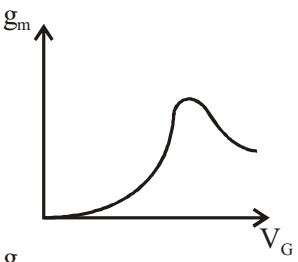
(c) P-3,Q-4, R-1, S-2

(d) P-3,Q-2, R-1, S-4

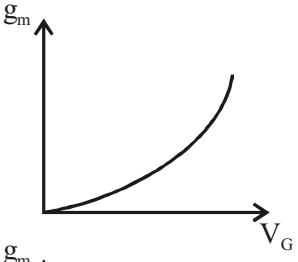
GATE(EC/2007/2M)

Q.16 The measured transconductance g_m of an NMOS transistor operating in the linear region is plotted aginst the gate voltage V_G at a constant drain voltage V_P. Which of the following figures represents the expected dependence of g_m on V_G ?

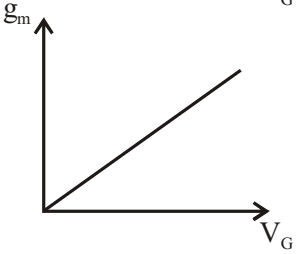
(a)



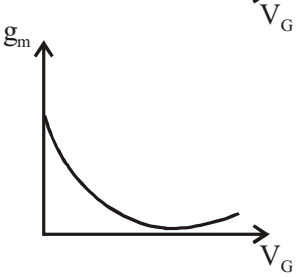
(b)



(c)



(d)



GATE(EC/2008/2M)

Q.17 The drain current of a MOSFET in saturation is given by $I_D = K (V_{GS} - V_T)^2$ where K is a constant. The magnitude of the transconductance g_m is

(a) $\frac{K(V_{GS}-V_T)^2}{V_{DS}}$ (b) $2K(V_{GS}-V_T)$

(c) $\frac{I_D}{V_{GS}V_{DS}}$ (d) $\frac{K(V_{GS}-V_T)^2}{V_{GS}}$

GATE(EC/2008/1M)

Q.18 Consider the following two statements about the internal conditions in an n-channel MOSFET operating in the active region.

S1: The inversion charge decreases from source to drain

S2: The channel potential increases from source to drain

Which of the following is correct ?

(a) Only S2 is true

(b) Both S1 and S2 are false.

(c) Both S1 and S2 are ture, but S2 is not a reason for S1

(d) Both S1 and S2 are true, and S2 is a reason for S1

GATE(EC/2009/2M)

Q.19 At room temperature, a possible value for the mobility of electrons in the inversion layer of a silicon n-channel MOSFET is

(a) 450 cm^2/V-s (b) 1350 cm^2/V-s

(c) 1800 cm^2/V-s (d) 3600 cm^2/V-s

GATE(EC/2010/1M)

Q.20 The source of a silicon ($n_i = 10^{10}$ per cm^3) n-channel MOS transistor has an area of 1 sq μm and a depth of 1μm.If the dopant density in the source is $10^{19}/cm^3$,the number of holes in the source region with the above volume is approximately

(a) 10^7 (b) 100

(c) 10 (d) 0

GATE(EC/2012/2M)

Q.21 In a MOSFET operating in the saturation region, the channel length modulation effect causes

(a) an increase in the gate-source capacitance

(b) a decrease in the transconductance

(c) a decrease in the unity - gain cutoff frequency

(d) a decrease in the output resistance

GATE(EC/2013/1M)

Q.22 If fixed positive charges are present in the gate oxide of an n-channel enhancement type MOSFET, it will lead to

(a) a decrease in the threshold voltage (b) channel length modulation

(c) an increase in substrate leakage current (d) an increase in accumulation capacitance

GATE(EC-I/2014/1M)

Q.23 A depletion type N-channel MOSFET is biased in its linear region for use as a voltage controlled

resistor. Assume threshold voltage V_{TH} = –0.5 V, V_{GS} = 2.0 V, V_{DS} = 5 V, W/L = 100, C_{OX} = 10^{-8} F/cm^2 and μ_n = 800 cm^2/V-s. The value of the resistance of the voltage controlled resistor (in Ω) is _____

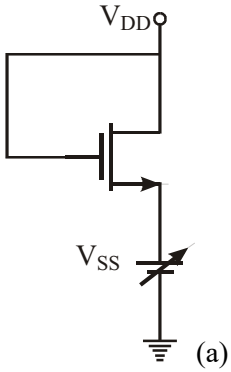
GATE(EC-I/2014/2M)

Q.24 In MOSFET fabrication, the channel length is defined during the process of

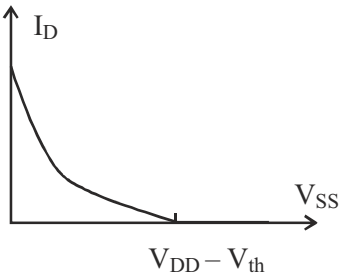
(a) isolation oxide growth
(b) channel stop implantation
(c) poly-silicon gate patterning
(d) lithography step leading to the contact pads

GATE(EC-III/2014/1M)

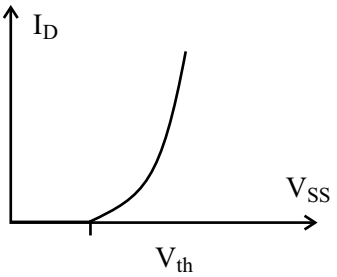
Q.25 For the N MOSFET in the circuit shown, the threshold voltage is V_{th}, where $V_{th} > 0$. The source voltage V_{SS} is varied from 0 to V_{DD}. Neglecting the channel length modulation, the drain current I_D as a function of V_{SS} is represented by



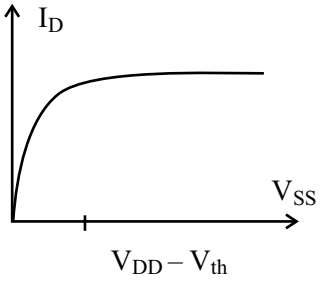
(a)



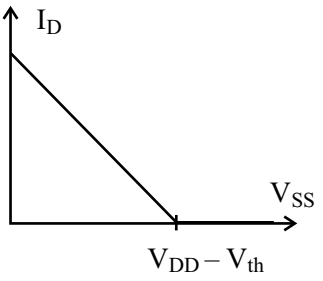
(b)



(c)



(d)



GATE(EC-I/2015/2M)

Q.26 Which one of the following processes is preferred to form the gate dielectric (SiO_2) of MOSFETs?

(a) Sputtering
(b) Molecular beam epitaxy
(c) Wet oxidation
(d) Dry oxidation

GATE(EC-III/2015/1M)

Q.27 A long-channel NMOS transistor is biased in the linear region with V_{DS} = 50 mV and is used as a resistance. Which one of the following statements is NOT correct?

(*a*) If the device width W is increased, the resistance decreases.

(*b*) If the threshold voltage is reduced, the resistance decreases.

(*c*) If the device length L is increased, the resistance increases.

(*d*) If V_{GS} is increased, the resistance increases.

GATE(EC-II/2016/1M)

Q.28 Consider the following statements for a metal oxide semiconductor field effect transistor (MOSFET):

P: As channel length reduces, OFF-state current increases.

Q: As channel length reduces, output resistance increases.

R: As channel length reduces, threshold voltage remains constant.

S: As channel length reduces, ON current increases.

Which of the above statements are INCORRECT?

(a) P and Q (b) P and S

(c) Q and R (d) R and S

GATE(EC-I/2016/1M)

Q.29 Consider an n-channel MOSFET having width W, length L, electron mobility in the channel μ_n and oxide capacitance per unit area C_{ox}. If gate-to-source voltage V_{GS}= 0.7V, drain-to-source voltage V_{DS}= 0. 1V, $(\mu_n C_{ox}) = 100\ \mu A/V^2$, threshold voltage V_{TH} = 0.3 V and (W/L) = 50, then the transconductance gm (in mA/V) is _____.

GATE(EC-II/2017/1M)

Q.30 An n-channel enhancement mode MOSFET is biased at $V_{GS} > V_{TH}$ and $V_{DS} > (V_{GS} - V_{TH})$ where V_{GS} is the gate-to-source voltage, V_{DS} is the drain-to-source voltage and V_{TH} is the threshold voltage. Considering channel length modulation effect to be significant, the MOSFET behaves as a

(a) voltage source with zero output impedance

(b) voltage source with non-zero output impedance

(c) current source with finite output impedance

(d) current source with infinite output impedance

GATE(EC-II/2017/1M)

Q.31 Two n-channel MOSFETs, T_1 and T_2, are identical in all respects except that the width of T_2 is double that of T_1. Both the transistors are biased in the saturation region of operation, but the gate overdrive voltage $(V_{GS} - V_{TH})$ of T_2 is double that of T_1, where V_{GS} and V_{TH} are the gate – to – source voltage and threshold voltage of the transistors, respectively. If the drain current and transconductance of T_1 are I_{D1} and g_{m1} respectively, the corresponding values of these two parameters for T_2 are

(a) $8I_{D1}$ and $2g_{m1}$ (b) $8I_{D1}$ and $4g_{m1}$

(c) $4I_{D1}$ and $4g_{m1}$ (d) $4I_{D1}$ and $2g_{m1}$

GATE(EC-II/2017/2M)

Q.32 Given, V_{gs} is the gate-source voltage, V_{ds} is the drain source voltage, and V_{th} is the threshold voltage of an enhancement type NMOS transistor, the conditions for transistor to be biased in saturation are

(a) $V_{gs} < V_{th}$; $V_{ds} \geq V_{gs} - V_{th}$ (b) $V_{gs} > V_{th}$; $V_{ds} \geq V_{gs} - V_{th}$

(c) $V_{gs} > V_{th}$; $V_{ds} \le V_{gs} - V_{th}$ (d) $V_{gs} < V_{th}$; $V_{ds} \le V_{gs} - V_{th}$

GATE(EE/2019/1M)

Q.33 An n-channel JFET has a pinch-off voltage of $V_p = -5$ V, V_{DS} (max) = 20 V, and g_m = 2mA/V. The minimum 'ON' resistance is achieved in the JEFT for

(a) $V_{GS} = -7V$ and $V_{DS} = 0V$ (b) $V_{GS} = 7V$ and $V_{DS} = 0V$

(c) $V_{GS} = 0V$ and $V_{DS} = 20V$ (d) $V_{GS} = -7V$ and $V_{DS} = 20V$

GATE(EC/1992/2M)

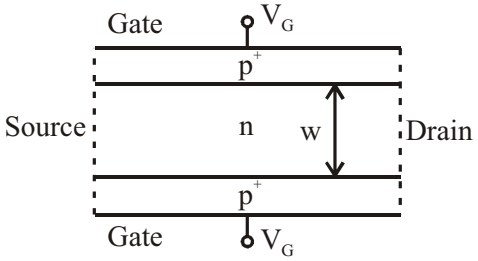
Q.34 The action of JFET in its equivalent circuit can best be represented as a

(a) Current Controlled Voltage Source (b) Current Controlled Voltage Source

(c) Voltage Controlled Voltage Source (d) Voltage Controlled Current Source

GATE(EC/2003/2M)

Q.35 The cross section of a JFET is shown in the following figure. Let V_G be – 2V and let V_P be the initial pinch-off voltage. If the width w is doubled (with other geometrical parameters and doping levels remaining the same), then the ratio between the mutual transconductances of the initial and the modified JFET is



(a) 4 (b) $\frac{1}{2}\left(\frac{1-\sqrt{2/V_P}}{1-\sqrt{1/(2V_P}}\right)$

(c) $\frac{1}{2}\left(\frac{1-\sqrt{2/V_P}}{1-\sqrt{1/(2V_P}}\right)$ (d) $\frac{1-(2/\sqrt{V_P})}{1-(1/2\sqrt{V_P})}$

GATE(EC/2008/2M)

Q.36 Which of the following can be considered to be the advantage of FET amplifiers as compared to BJT amplifiers?

1. Higher input impedance
2. Good bias stability
3. Higher gain-bandwidth product
4. Lower noise figure

Select the correct answer using the codes given below:

Codes:

(a) 1,2 and 3 (b) 1,2 and 4

(c) 2,3 and 4 (d) 1,3 and 4

Q.37 Which of the following can be considered to be the advantage of FET amplifiers as compared to BJT

amplifiers?

1. Higher input impedance
2. Good bias stability
3. Higher gain-bandwidth product
4. Lower noise figure

Select the correct answer using the codes given below:

Codes:

(a) 1,2 and 3 (b) 1,2 and 4

(c) 2,3 and 4 (d) 1,3 and 4

GATE(EC/1990/2M)

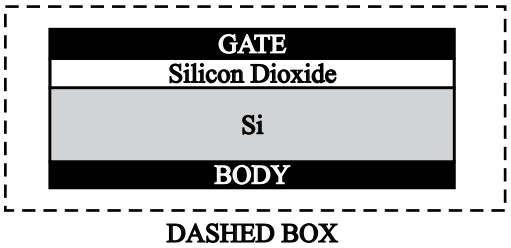
Q.38 The "Pinch off" voltage of a JFET is 5.0 volts. Its "Cut off" voltage is

(a) $(5.0)^{1/2}$V (b) 2.5 V

(c) 5.0 V (d) $(5.0)^{3/2}$V

GATE(EC/1990/2M)

Q.39 The cross-section of a metal-oxide-semiconductor structure is shown schematically. Starting from an uncharged condition, a bias of +3 V is applied to the gate contact with respect to the body contact. The charge inside the silicon dioxide layer is then measured to be +Q. The total charge contained within the dashed box shown, upon application of bias, expressed as a multiple of Q (absolute value in Coulombs, rounded off to the nearest integer) is _____.



GATE(EE/2020/1M)

Q.40 For an n-channel silicon MOSFET with 10 nm gate oxide thickness, the substrate sensitivity $\left(\partial V_T / \partial V_{BS}\right)$ is found to be 50 mV/V at a substrate voltage $|V_{BS}| = 2$ V, where V_T is the threshold voltage of the MOSFET. Assume that, $|V_{BS}| \gg 2\Phi_B$, where $q\Phi_B$ is the separation between the Fermi energy level E_F and the intrinsic level E_i in the bulk. Parameters given are

Electron charge (q) = 1.6×10^{-19} C

Vacuum permittivity (ε_0) = 8.85×10^{-12} F/m

Relative permittivity of silicon (ε_{Si}) = 12

Relative permittivity of oxide (ε_{ox}) = 4

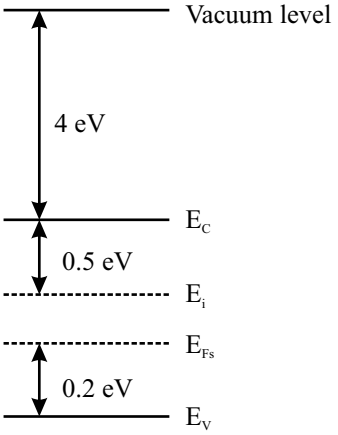
The doping concentration of the substrate is

(a) 7.37×10^{15} cm^{-3} (b) 4.37×10^{15} cm^{-3}

(c) 2.37×10^{15} cm^{-3} (d) 9.37×10^{15} cm^{-3}

GATE(EC/2021/2M)

Q.41 The band diagram of a p-type semiconductor with a band-gap of 1 eV is shown. Using this semiconductor, a MOS capacitor having V_{Th} of –0.16 V, C'_{ox} of 100 nF/cm^2 and a metal work function of 3.87 eV is fabricated. There is no charge within the oxide. If the voltage across the capacitor is V_{Th}. the magnitude of depletion charge per unit area (in C/cm^2) is



(a) 1.70×10^{-8} (b) 0.52×10^{-8}

(c) 1.41×10^{-8} (d) 0.93×10^{-8}

GATE(EC/2020/2M)

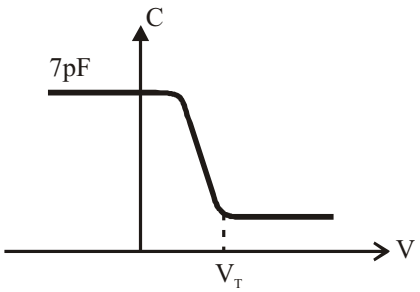
❐❐❐

ANSWERS & EXPLANATIONS

Q.1 ***Ans.(a)***

In accumulation mode of MOS capacitor, with p-substrate, the dominant charge is due to presence of holes and in inversion mode of same capacitor the dominant charge is due to electrons. The capacitor is in accumulation mode when metal plate is applied negative potential with respect to semi conductor and inversion mode is observed when metal plate is given positive potential w.r.t. semiconductor layer.

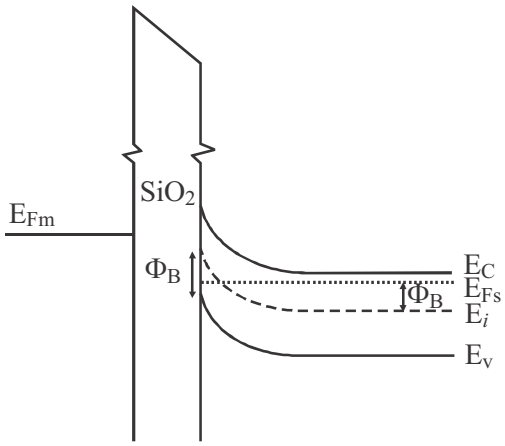
Q.2 ***Ans.(c)***



Statement, S_1 : From given characteristics it is observed that capacitance minimum beyond positive value of voltage V. This voltage is called threshold voltage. The threshold voltage is positive only for a p-substrate. Hence given MOS capacitor has p-substrate. So, given statement S_1 is false.

Statement, S_2 : If positive charges are introduced in oxide layer the threshold voltage required for inversion of charges below oxide layer is reduced because positive charges exert additional attractive force on electrons of p-substrate. Therefore, C-V plot will shift to the left when positive charges are introduced in oxide. So, given statement S_2 is true.

Q.3 **Ans. (*a*)**



It is observed from above diagram that the intrinsic Fermi level is in bulk of substrate is below the actual Fermi level and it is above the actual Fermi level at the oxide-semiconductor interface which

is possible only in inverse mode of operation of the MOS capacitor.

Q.4 Ans. 1.55:1.65

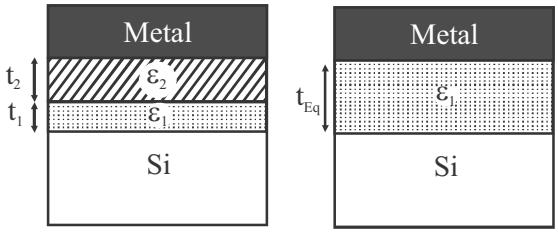
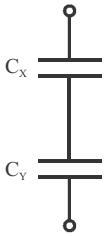


Figure I Figure II

The equivalent capacitance of combination in Figure I is two capacitors connected in seires as under,



The equivalent capacitance of series combination of capacitors is given by,

$$C_{eq1} = \frac{C_X C_Y}{C_X + C_Y} \quad \text{.....(i)}$$

If capacitor has unit are then capacitances of material X & Y per unit area are given by,

$C_X = \frac{\varepsilon_1 \varepsilon_o}{t_1}$ = Capacitance per unit area of X

$C_Y = \frac{\varepsilon_2 \varepsilon_o}{t_2}$ = Capacitance per unit area of Y

The capacitance per unit area of capacitor of Figure II is given by,

$$C_{eq2} = \frac{\varepsilon_1 \varepsilon_o}{t_{Eq}} \quad \text{.....(ii)}$$

If both Figure I and Figure II are having equal capacitances the from equations (i) and (ii), we have,

$$\frac{\varepsilon_1 \varepsilon_o}{t_{Eq}} = \frac{C_X C_Y}{C_X + C_Y}$$

$$\Rightarrow \quad \frac{\varepsilon_1 \varepsilon_o}{t_{Eq}} = \frac{\frac{\varepsilon_1 \varepsilon_o}{t_1} \times \frac{\varepsilon_2 \varepsilon_o}{t_2}}{\frac{\varepsilon_1 \varepsilon_o}{t_1} + \frac{\varepsilon_2 \varepsilon_o}{t_2}}$$

$$\Rightarrow \quad t_{Eq} = \frac{\varepsilon_1 t_2 + \varepsilon_2 t_1}{\varepsilon_2}$$

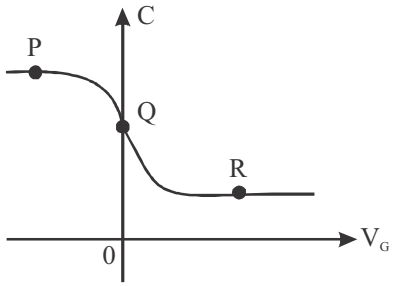
Given, $t_1 = 1$ nm, $\varepsilon_1 = 4$, $t_2 = 3$ nm and $\varepsilon_2 = 20$

$$\Rightarrow \quad t_{Eq} = \frac{4\times 3 + 20\times 1}{20}\text{nm}$$

$$\Rightarrow \quad t_{Eq} = 1.6 \text{ nm}$$

Q.5 ***Ans.(b)***

Given C-V curve of MOS capacitor,



(i) When V is negative the MOS capacitor works in Accumulation mode at 'P'.

(ii) When V = 0, the MOS capacitor offers flat band at 'Q'.

(iii) Finally MOS capacitor works in inversion mode with V > 0 at 'R'.

Q.6 ***Ans.(b,c)***

Reverse saturation current in BJT double for every 10°C rise in temperature. β of BJT also increases with increase in temperature. Since $I_C = \beta I_B + (1 + \beta) I_{CO}$, therefore I_C, increases with increase in temperature. A MOSFET has positive temperature coefficient so its drain resistance increases with increase in temperature hence drain current decreases with increase in temperature.

Q.7 ***Ans.(a)***

The threshold voltage of n-channel MOSFET can be increased by increasing the channel dopant concentration or by increasing the oxide thickness.

Note :- *Methods of reducing V_{TH} :*

i) By using S_i with <100> structure instead of <111> structure.

ii) By using layer of (Si_3N_4 + SiO_2) instead of SiO_2 alone

iii) Poly crystalline Si doped with boron is used as gate electrode instead of Al.

iv) By reducing thickness of oxide layer which in turn increases oxide capacitance.

v) By decreasing doping concentration in substrate.

vi) By ion implantation near drain and source terminals

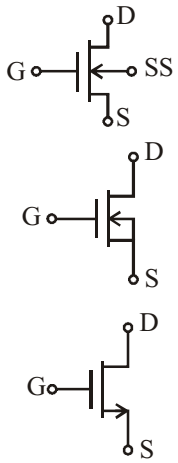
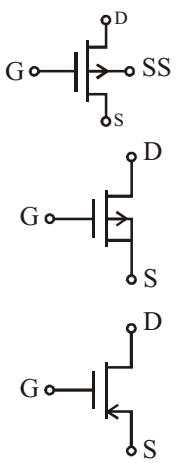
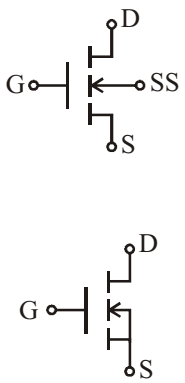
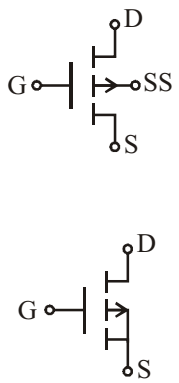
vii) By connecting the source at lower potential than Bulk.

Q.8 Ans.(a)

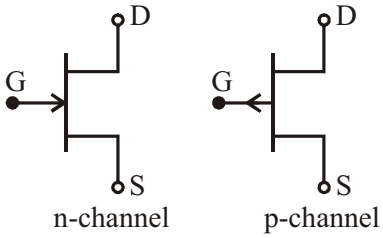
MOSFET behaves like a closed switch when it is operated in ohmic region of its drain characteristics. In ohmic region it offers a finite resistance. So, the MOSFET switch in its on-state may be considered equivalent to a resistor.

Q.9 Ans.(a)

i) Symbols of MOSFETs :

	Type of MOSFET	
	n-channel	**p-channel**
DEPLETION TYPE		
ENHANCEMENT TYPE		

ii) Symbols of JFETs :–



Q.10 ***Ans.(b)***

Effective channel length of a MOSFET in saturation decreases with increase in drain voltage.

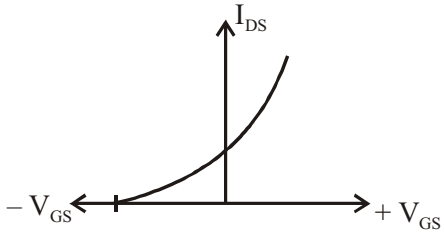
Q.11 ***Ans.(b)***

MOSFET can be used as voltage controlled capacitor.

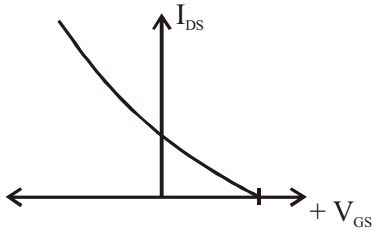
Q.12 ***Ans.(b)***

Transfer characteristics of MOSFETS :

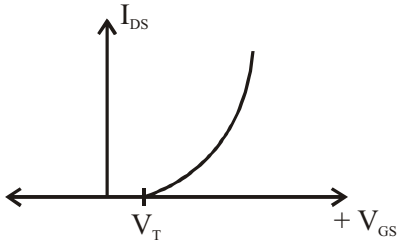
Case-I: n-channel depletion mode



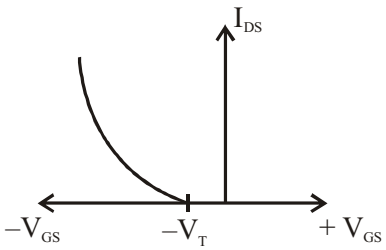
Case-II: p-channel depletion mode



Case-III: n-channel enhancement mode



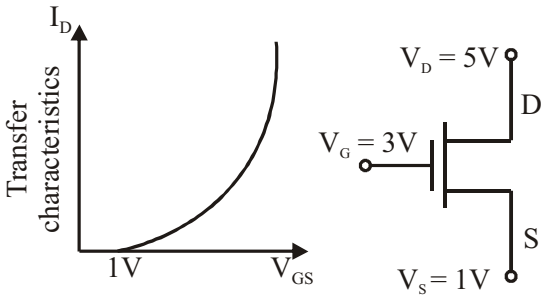
Case-IV p-channel enhancement mode



Q.13 Ans.(d)

The threshold voltage of n-channel enhancement type MOSFET increases if source is connected at higher potential than Bulk.

Q.14 Ans.(c)



From transfer characteristic threshold voltage of MOSFET,

$$V_T = 1V$$

From MOSFET voltages,

$$V_{GS} = V_G - V_S = 3 - 1 = 2V$$

$$V_{GS} - V_T = 2 - 1 = 1\ V$$

Also, $$V_{DS} = V_D - V_S = 5 - 1 = 4V$$

MOSFET operates in saturation region when $V_{DS} > (V_{GS} - V_T)$

Since given V_{DS} is more than $(V_{GS} - V_T)$, therefore, MOSFET must be operating in saturation region of output characteristic.

Q.15 Ans.(c)

I) BJT exhibits early effect

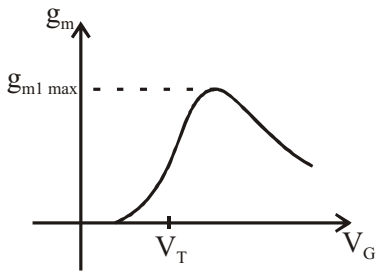
II) MOS capacitor has flat band voltage.

III) LASER diode exhibit population inversion

IV) JFET has a pinch voltage

***Q.16* Ans.(a)**

Variation of transconductance of NMOS as a function of gate voltage is as shown below



Q.17 **Ans.(b)**

Given, $I_D = K(V_{GS} - V_T)^2$

The transconductance of MOSFET is defined by

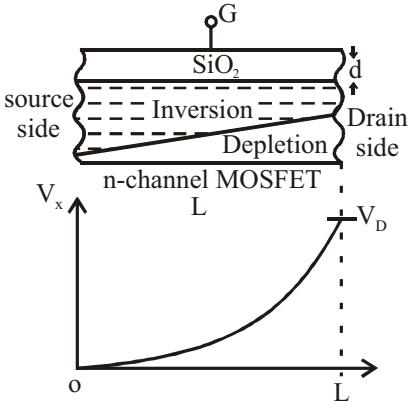
$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=\text{constant}}$$

$$\Rightarrow \quad g_m = \frac{\partial}{\partial V_{GS}}[K(V_{GS} - V_T)^2]$$

$$\Rightarrow \quad g_m = 2K[V_{GS} - V_T]$$

Q.18 ***Ans.(d)***

The inversion charge decreases in n-channel MOSFET from source to drain because the channel potential increases from source to drain.



Q.19 ***Ans.(a)***

The mobility of electron in n-type Si semiconductor is 1350 $cm^2/V\text{-}s$ but mobility of carriers decreases with increase in electric field. The electric field in inversion layer of n-channel MOSFET is high. So mobility of electrons falls below 1350 $cm^2/V\text{-}s$. So, option (a) is correct.

Q.20 **Ans.(d)**

In n-channel MOS transistor the source region is also n-type and in n-type material the number holes are equal to the number of intrinsic electrons.

Volume of the source = $1 \times 10^{-12} \times 1 \times 10^{-6} = 10^{-18}\ m^3$

Density of intrinsic electrons,

$n_i = 10^{10} \times 10^6 / m^3 = 10^{16}$ per m^3

Number of intrinsic electrons $= 10^{16} \times 10^{-18}$

$= 10^{-2} = 0.01$

Number of holes = Number of intrinsic electrons

$= 0.01 \approx 0$

Q.21 Ans.(d)

When gate to source voltage of n – MOSFET is increased the effective channel length is reduced which is called channel length modulation . The channel length modulation has following effects,

i. Output resistance (drain resistance) of MOSFET reduces.
ii. High frequency response of MOSFET is improved. So, unity given cut off frequency is increased.
iii. Trans conductance of MOSFET is increased.
iv. Switching speed is increased.

Q.22 Ans.(a)

If fixed positive charges are present in the gate oxide of an n-channel enhancement type MOSFET, it will lead to a decrease in the threshold voltage and increase in Flat band voltage. The flat band voltage becomes more negative in n-channel MOSFET.

Q.23 Ans.: 499 to 501

The n-channel MOSFET can be used as a voltage controlled resistor when it is operated in Ohmic region. The drain current in ohmic region of operation is given by,

$$I_D = \frac{\mu_n C_{ox} \mathcal{W}}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

The channel conductance in ohmic region is defined as,

$$g_D = \frac{\partial I_D}{\partial V_{DS}}$$

$$\Rightarrow \quad g_D = \frac{\mu_n C_{ox} \mathcal{W}}{L} \cdot \left[(V_{GS} - V_T) - V_{DS}\right]$$

$$\Rightarrow \quad g_D = 800 \times 10^{-8} \times 100\ [(2 - (0.5) - 5]$$

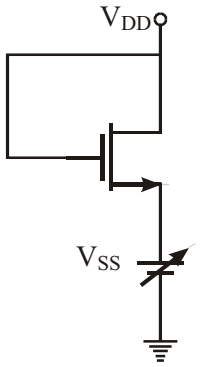
$$g_D = 2000 \times 10^{-8} \times 100 = -\frac{1}{500}$$

Channel resistance, $|r_D| = \left|\frac{1}{g_D}\right| = 500\,\Omega$

Q.24 Ans (c)

In MOSFET fabrication, the channel length is defined during the process of poly-silicon gate patterning.

Q.25 **Ans. (*a*)**



Since drain is shorted with gate terminal, therefore,

If $V_{DS} = V_{GS}$ then $V_{DS} < V_{GS} - V_{th}$.

When $V_{DS} < V_{GS} - V_{th}$, the MOSFET operates in ohmic region of operation with drain current given by,

$$I_D = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} + \frac{1}{2}V_{DS}^2\right]$$

Putting, $V_{GS} = V_{DS}$ in above equation, we have,

$$I_D = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L}\left[(V_{DS} - V_{th})V_{DS} + \frac{1}{2}V_{DS}^2\right]$$

From the circuit diagram given above,

$$V_{DS} = V_{DD} - V_{SS}$$

Case-I: When $V_{SS} = 0$, $V_{DS} = V_{DD} - 0 = V_{DD}$

$$\Rightarrow I_D = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L}\left[(V_{DD} - V_{th})V_{DD} + \frac{1}{2}V_{DD}^2\right] \quad \text{.....(i)}$$

Case-II: When $V_{SS} = V_{DD}$

$$V_{DS} = V_{DD} - V_{DD} = 0$$

$$\Rightarrow I_D = 0$$

It is observed from above two cases that when voltage V_{SS} is changed from 0 to V_{DD} the drain current varies non-linearly from value given by equation (i) to zero.

So, option (a) is correct choice.

Q.26 ***Ans. (d)***

Dry oxidation is preferred to form the gate dielectric (SiO_2) of MOSFETs.

Q.27 ***Ans. (d)***

The drain current in ohmic region of drain characteristics of MOSFET is given by

$$I_D = \frac{\mu_n C_{ox} \mathcal{W}}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

Conductance of channel,

$$g_D = \frac{\partial I_D}{\partial V_{DS}} = \frac{\mu_n C_{ox} \mathcal{W}}{L}\left[(V_{GS} - V_T) - V_{DS}\right]$$

$$r_D = \frac{1}{g_D} = \frac{1}{\frac{\mu_n C_{ox} \mathcal{W}}{L}\left[(V_{GS} - V_T) - V_{DS}\right]}$$

Observation :

(i) Channel resistance increases when L is increased

(ii) Channel resistance decreases when channel width W is increased.

(iii) Channel resistance decreases when voltage V_{GS} is increased

So, option (d) is not correct

Q.28 **Ans. (*c*)**

When channel length of MOSFET is reduced,

Q: output resistance decreases.

R: threshold voltage remains unchanged

Q.29 ***Ans. : 0.45 to 0.55***

When $V_{DS} < V_{GS} - V_{TH}$, the MOSFET works in ohmic region.

Given, V_{GS} =0.7V, V_{DS} = 0.1V ,V_{TH} = 0.3

$\therefore$ $V_{GS} - V_{TH} = 0.7 - 0.3 = 0.4$

Here, $V_{DS} < V_{GS} - V_{TH}$, so given MOSFET works in ohmic region for given V_{DS} and V_{GS}. Two drain current in ohmic region is given by,

$$I_D = \frac{\mu_n C_{ox} \mathcal{W}}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{GS}^2\right]$$

Trans conductance in given as,

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\mu_n C_{ox} \mathcal{W}}{L} \cdot V_{DS}$$

Given, $\mu_n C_{ox} = 100\mu A/V^2$

and $\frac{W}{L} = 50, V_{DS} = 0.1V$

$\therefore$ $g_m = 100 \times 10^{-6} \times 50 \times 0.1$

$\Rightarrow$ $g_m = 0.5$ mA/V

Q.30 ***Ans. (c)***

An n-channel enhancement mode MOSFET operates in saturation region when it is biased at $V_{GS} > V_{TH}$ and $V_{DS} > (V_{GS} - V_{TH})$. If channel length modulation effect is significant it behaves current source with finite output impedance.

Q.31 ***Ans. (b)***

The drain current of n-channel MOSFET in saturation region is given by,

$$I_D = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_T)^2 \quad \text{....(i)}$$

Given $W_2 = 2W_1$ .....(ii)

$V_{GS2} - V_{T2} = 2\,(V_{GS1} - V_{T1})$ ....(iii)

From equation (i)

$$\frac{I_{D2}}{I_{D1}} = \frac{W_2}{W_1} \times \frac{(V_{GS2} - V_{T2})^2}{(V_{GS1} - V_{T1})^2}$$

$$\Rightarrow \quad \frac{I_{D2}}{I_{D1}} = \frac{2W_1}{W_1} \times \frac{\left[2(V_{GS1} - V_{T1})\right]^2}{V_{GS1} - V_{T1}}$$

$$\Rightarrow \quad I_{D2} = 8\, I_{D1}$$

Transconductance in saturation region of MOSFET,

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\mu_m C_{ox} W}{L}(V_{GS} - V_T)$$

$$\Rightarrow \quad \frac{g_{m2}}{g_{m1}} = \frac{W_2 (V_{GS2} - V_{T2})}{W_1 (V_{GS1} - V_{T1})}$$

$$\Rightarrow \quad \frac{g_{m2}}{g_{m1}} = \frac{2W_1 \times 2(V_{GS1} - V_{T1})}{W_1 (V_{GS1} - V_{T1})}$$

$$\Rightarrow \quad g_{m2} = 4\, g_{m1}$$

Q.32 ***Ans.(b)***

NMOS works in saturation region when following two conditions are satisfied.

(i) $V_{GS} > V_{TH}$

(ii) $V_{DS} \geq V_{GS} - V_{TH}$

Note : *I. For saturation region,* $V_{GS} > V_{TH}$

$V_{DS} \geq V_{GS} - V_{TH}$

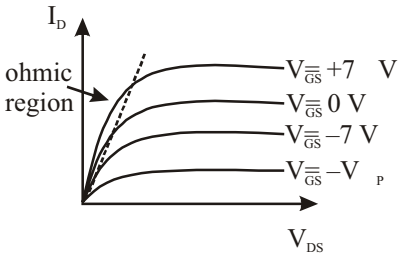
II. For ohmic region, $V_{GS} > V_{TH}$

$V_{DS} \le V_{GS} - V_{TH}$

III. For cutoff region, $V_{GS} < V_{TH}$

Q.33 Ans.(b)

A JFET behaves like ohmic device in ohmic region of operation. From drain characteristics of JFET it is clear that the device operates in ohmic region when voltage V_{DS} is very small, ideally, $V_{DS} = 0$. The slope of characteristics increases with change in V_{GS} from negative to positive. So the given JFET offers minimum 'ON' resistance when V_{GS} is positive and large. i.e. at $V_{as} = +7$ v and $V_{DS} = 0$V



Q.34 Ans.(d)

The action of JEFT in its equivalent circuit can be represented as voltage controlled current source.

Q.35 Ans.(b)

Transconductance of JFET in saturation region is given by,

$$g_m(sat) = G_o\left[1-\left(\frac{V_G}{V_P}\right)^{1/2}\right]$$

Where, $G_o = \dfrac{2aZ}{\rho L}$ = conductance with no gate voltage

L $\rightarrow$ Length of channel

a $\rightarrow$ Half width of channel

Z $\rightarrow$ Depth of channel

ρ $\rightarrow$ Resistivity of material of channel

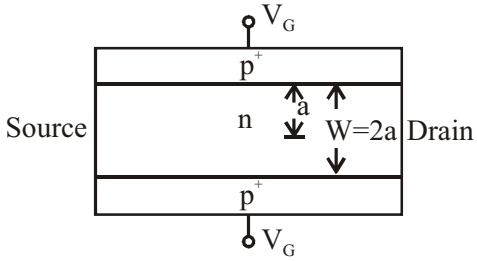
w $\rightarrow$ Width of channel

$$\Rightarrow \quad \frac{g_{m2}}{g_{m1}} = \frac{a_2}{a_1}\cdot\frac{1-\left(\dfrac{-V_G}{V_{P2}}\right)^{1/2}}{1-\left(\dfrac{-V_G}{V_{P1}}\right)^{1/2}}$$

Given, $w_2 = 2w_1$

or $a_2 = 2a_1$

and $V_G = -2$ V



$\Rightarrow$ Also pinch off voltage

$$V_P = \frac{qa^2N_D}{2\epsilon}$$

$\Rightarrow$ $$V_P \propto a^2$$

$$\frac{V_{P2}}{V_{P1}} = \frac{a_2^2}{a_1^2} = 4$$

$\Rightarrow$ $$V_{P2} = 4\,V_{P1} = 4\,V_P$$

$\Rightarrow$ $$\frac{g_{m1}}{g_{m2}} = \frac{a_1}{a_2}\cdot\frac{1-\left(\frac{2}{V_{P1}}\right)^{1/2}}{1-\left(\frac{2}{V_{P2}}\right)^{1/2}} = \frac{1}{2}\cdot\frac{1-\left(\frac{2}{V_P}\right)^{1/2}}{1-\left(\frac{2}{4V_P}\right)^{1/2}} = \frac{1}{2}\left[\frac{1-\left(\frac{2}{V_P}\right)^{1/2}}{1-\left(\frac{1}{2V_P}\right)^{1/2}}\right]$$

Q.36 Ans.(b)

Advantage of FET amplifiers over BJT amplifiers:

i) Higher input impedance
ii) Good bias stability
iii) Lower noise figure or less noisy.
iv) No secondary breakdown
v) Suitable for parallel operation
vi) Better switching speed
vii) Lower offset voltage, so it is better signal chopper

Disadvantages of FET over BJT amplifiers:

i) Lower gain bandwidth product
ii) Higher on-state resistance so higher on state losses.
iii) Lower power rating

Q.37 Ans.(b)

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Q.38 Ans.(c)

Pinch off voltage,

$$V_P = 5.0\ V$$

At cutoff the gate to source voltage of JFET is equal to pinch off voltage.

$$\therefore \quad V_{GS(OFF)} = V_P$$

$$\Rightarrow \quad V_{GS(OFF)} = 5.0\ V$$

Q.39 Ans(0 to 0)

Application of positive potential at Gate terminal of metal-oxide-semiconductor structure shown in figure induces both negative and positive charges. Therefore, net charge on structure as a whole is always zero.

Q.40 Ans.(a)

The change in threshold voltage due to substrate body effect is given by,

$$\Delta V_T = \frac{\sqrt{2\varepsilon_s q N_A}}{C_i}\left[\left(2\phi_F + |V_B|\right)^{1/2} - \left(2\phi_F\right)^{1/2}\right]$$

Where, V_B is substrate bias voltage.

$$C_i = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{4 \times 8.85 \times 10^{-14}}{10 \times 10^{-7}}$$

$$\therefore \quad \frac{\partial V_T}{\partial V_B} = \frac{1}{2}\frac{\sqrt{2 \in_s qN_A}}{C_i}\left(2\phi_F + |V_B|\right)^{-\frac{1}{2}}$$

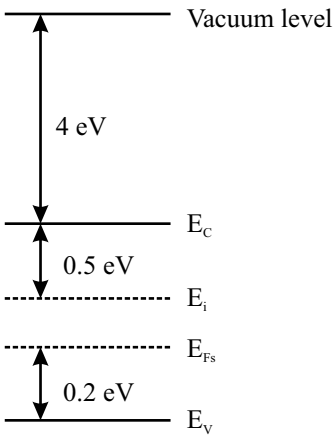
If $2\phi_F << |V_B|$,

$$\therefore \quad \frac{\partial V_T}{\partial V_B} = \frac{1}{2}\frac{\sqrt{2\varepsilon_s q N_A}}{C_i} \times \frac{1}{\sqrt{|V_B|}}$$

$$\Rightarrow \quad 50 \times 10^{-3} = \frac{\sqrt{2 \times 12 \times 8.85 \times 10^{-14} \times 1.6 \times 10^{-19} N_A}}{2 \times 4 \times 8.85 \times 10^{-14} / 10 \times 10^{-7}} \times \frac{1}{\sqrt{2}}$$

$\Rightarrow$ $N_A \approx 7.37 \times 10^{15}\ cm^{-3}$

Q.41 Ans(a)



From given energy level diagram work function of semiconductor,

$$\phi_s = X + \frac{E_g}{2} + (E_i - E_{Fs})$$

$$\phi_s = 4 + 0.5 + (0.5 - 0.2) = 4.8\ eV$$

Work function of metal, $\phi_m = 3.87\ eV$

Metal to semiconductor work function difference,

$$q\phi_{ms} = q\phi_m - q\phi_s = 3.87 - 4.8 = -0.93\ eV$$

$\Rightarrow$ $$\phi_{ms} = -\frac{0.93}{q} eV = -0.93V$$

Threshold voltage of MOS capacitor is given by,

$$V_{Th} = -\frac{(Q_{dT} + Q_x)}{C_{ox}} + 2\phi_F + \phi_{ms}$$

Where, Q_{dT} is depletion layer charge, C_{ox} oxide layer capacitance and Q_x is charge trapped in oxide layer.

Here, $Q_x = 0$ (given)

$\therefore$ $$V_{Th} = -\frac{Q_{dT}}{C_{ox}} + \phi_{ms} + 2\phi_F$$

From given energy diagram

$$q\phi_F = E_i - E_{Fs} = 0.5 - 0.2 = 0.3\ eV$$

$$\phi_F = 0.3\ V$$

Also given, $V_{Th} = -0.16\ V$

and $C_{ox} = 100\ nF/cm^2$

$$\Rightarrow \quad -0.16 = -\frac{Q_{dT}}{100\times10^{-9}} - 0.93 + 2\times0.3$$

$$\Rightarrow \quad \boxed{Q_{dT} = -1.7\times10^{-8}\,C/cm^{-2}}$$

❐❐❐

About the Author

Dr. Ram Niwas is from Indian Railways Services of Electrical Engineers. He obtained BE degree in Electronics and Power Engineering from NIT(VRCE), Nagpur in 1998, ME degree in Control and Instrumentation Engineering in 2003 and Ph.D in 2015 from IIT, Delhi. He worked with TATA Infotech from January 2000 to June 2000. From August 2000 to December 2001 he worked as lecturer in the Department of Electronics and Communication Engineering in Krishna Institute of Engg. & Tech. Ghaziabad, U. P. From December 2001 to August 2002 he worked in Bharat Sanchar Nigam Limited as Junior Telecom Officer(JTO). Author has vast experience of competitive examinations and has been mentoring the students for cracking various competitive and univsersity examinations for past several years. Author qualified IES examination twice in year 2001 and 2004.

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